TDA8933

Class-D audio amplifier

Rev. 01 — 15 May 2007 Preliminary data sheet

1. General description

The TDA8933 is a high efficiency class-D amplifier with low power dissipation.

The continuous time output power is 2×10 W in a stereo half bridge application (R_L = 8 Ω) or 1×20 W in a mono full bridge application (R_L =16 Ω). Due to the low power dissipation the device can be used without any external heat sink when playing music. Due to the implementation of Thermal Foldback (TF), even for high supply voltages and/or lower load impedances, the device will continue to operate with considerable music output power without the need for an external heat sink.

The device has two full differential inputs driving two independent outputs. It can be used in a mono full bridge configuration (Bridge-Tied Load (BTL)) or a stereo half bridge configuration (Single-Ended (SE)).

2. Features

- High efficiency
- Application without heat sink using thermally enhanced small outline package
- Operating voltage from 10 V to 36 V asymmetrical or ± 5 V to ± 18 V symmetrical
- Thermally protected
- Thermal foldback
- Current limiting to avoid audio holes
- Full short circuit proof to supply lines (using advanced current protection)
- Switchable internal / external oscillator (master-slave setting)
- No pop noise
- Low power dissipation
- Mono bridge-tied load (full bridge) or stereo single-ended (half bridge) application
- Full differential inputs

3. Applications

- Flat panel television sets
- Flat panel monitor sets
- Multimedia systems
- Wireless speakers
- Mini/micro systems
- Home sound sets

NXP founded by Philips

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
General; V_p = 25 V, f_{osc} = 320 kHz, T_{amb} = 25 °C unless specified otherwise						
V_P	supply voltage	asymmetrical supply	10	25	36	V
		symmetrical supply	5	12.5	18	V
I_P	supply current	Sleep mode	-	0.6	1.0	mA
$I_{q(tot)}$	total quiescent current	Operating mode; no load, no snubbers or filter connected	-	40	50	mA
Stereo SE channel						
$P_{o(RMS)}$	RMS output power	continuous time output power per channel [1]				
		R_L = 4 Ω; V_P = 17 V				
		THD+N = 0.5 %, f_i = 1 kHz	5.9	6.5	-	W
		THD+N = 0.5 %, f_i = 100 Hz	-	6.5	-	W
		THD+N = 10 %, f_i = 1 kHz	7.5	8.3	-	W
		THD+N = 10 %, f_i = 100 Hz	-	8.3	-	W
		R_L = 8 Ω; V_P = 25 V				
		THD+N = 0.5 %, f_i = 1 kHz	7.3	8.1	-	W
		THD+N = 0.5 %, f_i = 100 Hz	-	8.1	-	W
		THD+N = 10 %, f_i = 1 kHz	9.3	10.3	-	W
		THD+N = 10 %, f_i = 100 Hz	-	10.3	-	W
		short time output power per channel; THD+N = 10 %, see Figure 23 for details [2]				
		R_L = 8 Ω; V_P = 31 V				
		THD+N = 0.5 %	11.2	12.4	-	W
		THD+N = 10 %	14.1	15.7	-	W

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Table 1. Quick reference data *…continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Mono BTL channel						
$P_{o(RMS)}$	RMS output power	continuous time output power [1] THD+N = 10 %; f_i = 1 kHz				
		R_L = 8 Ω; V_P = 17 V				
		THD+N = 0.5 %, f_i = 1 kHz	11.9	13.2	-	W
		THD+N = 0.5 %, f_i = 100 Hz	-	13.2	-	W
		THD+N = 10 %, f_i = 1 kHz	15.4	17.1	-	W
		THD+N = 10 %, f_i = 100 Hz	-	17.1	-	W
		R_L = 16 Ω; V_P = 25 V				
		THD+N = 0.5 %, f_i = 1 kHz	14.9	16.5	-	W
		THD+N = 0.5 %, f_i = 100 Hz	-	16.5	-	W
		THD+N = 10 %, f_i = 1 kHz	18.9	21	-	W
		THD+N = 10 %, f_i = 100 Hz	-	21	-	W
		short time output power; [2] THD+N = 10 %, see Figure 35 for details				
		R_L = 16 Ω; V_P = 31 V				
		THD+N = 0.5 %	22.8	25.3	-	W
		THD+N = 10 %	28.8	32	-	W

[1] Output power is measured indirectly, based on R_{DSon} measurement.

[2] 2 layer application board (55 mm × 45 mm), 35 µm copper, FR4 base material in free air with natural convection.

5. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
TDA8933T	SO32	plastic small outline package; 32 leads; body width 7.5 mm	SOT287-1

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6. Block diagram

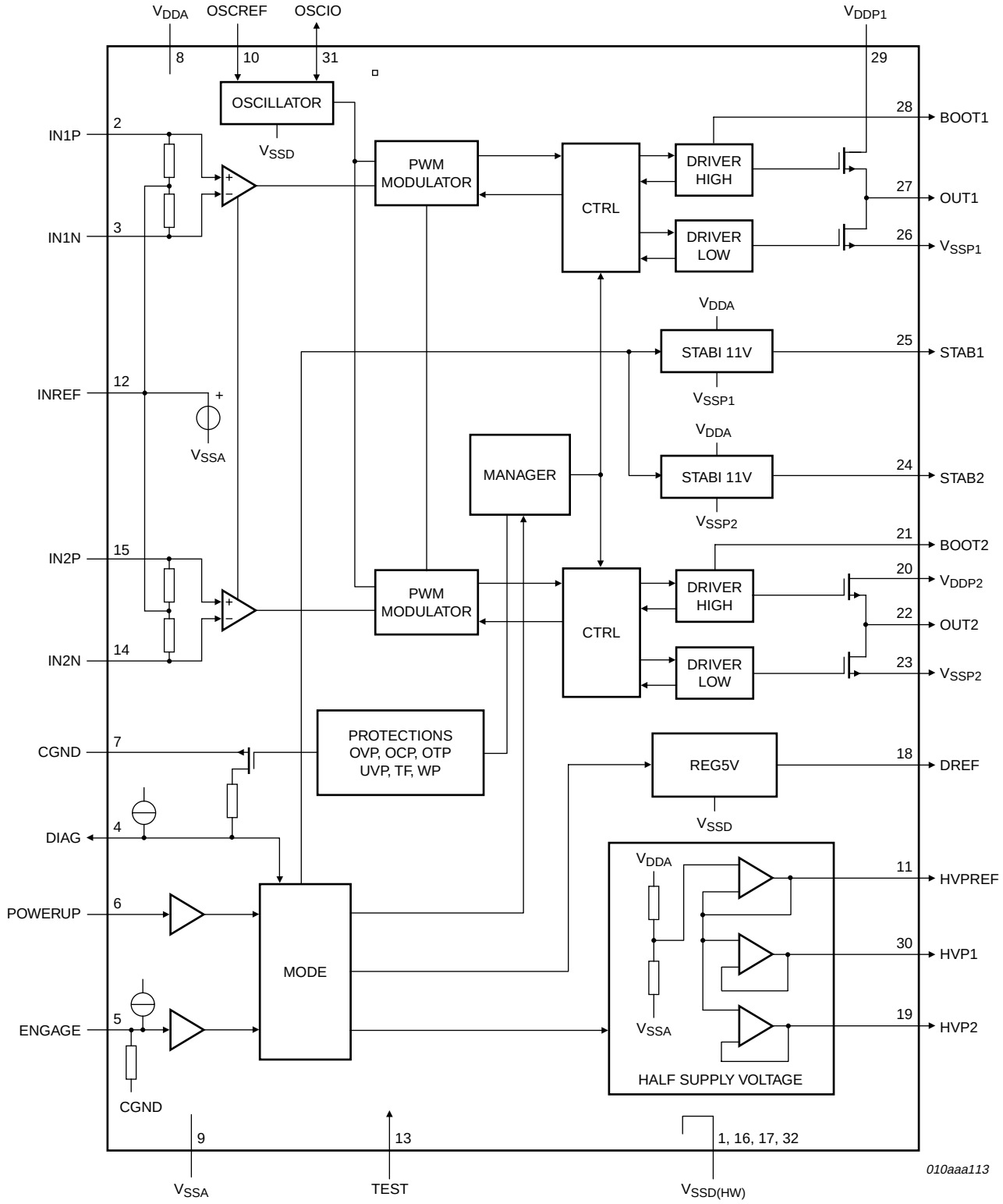


Fig 1. Block diagram

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7. Pinning information

7.1 Pinning

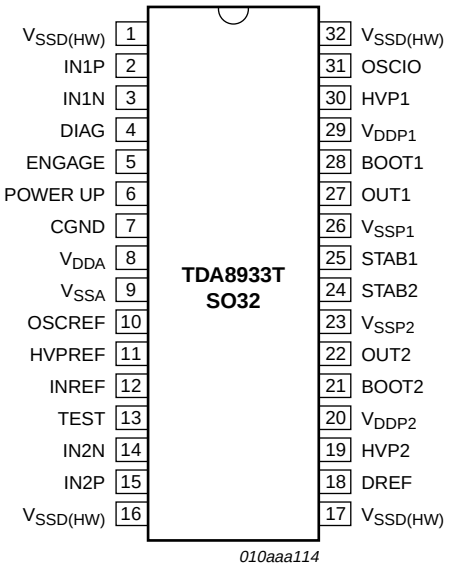


Fig 2. Pin configuration diagram

7.2 Pin description

Table 3. Pinning description

Symbol	Pin	Description
$V_{SSD(HW)}$	1	negative digital supply voltage and handle wafer connection
IN1P	2	positive audio input for channel 1
IN1N	3	negative audio input for channel 1
DIAG	4	diagnostic output; open-drain
ENGAGE	5	engage input to switch between Mute mode and Operating mode
POWERUP	6	power-up input to switch between Sleep mode and Mute mode
CGND	7	control ground; reference for POWERUP, ENGAGE and DIAG
V_{DDA}	8	positive analog supply voltage
V_{SSA}	9	negative analog supply voltage
OSCREF	10	input internal oscillator setting (only master setting)
HVPREF	11	decoupling of internal half supply voltage reference
INREF	12	decoupling for input reference voltage
TEST	13	test signal input; for testing purpose only
IN2N	14	negative audio input for channel 2
IN2P	15	positive audio input for channel 2
$V_{SSD(HW)}$	16	negative digital supply voltage and handle wafer connection
$V_{SSD(HW)}$	17	negative digital supply voltage and handle wafer connection
DREF	18	decoupling of internal (reference) 5 V regulator for logic supply

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Table 3. Pinning description …continued

Symbol	Pin	Description
HVP2	19	half supply output voltage 2 for charging single-ended capacitor for channel 2
V_{DDP2}	20	positive power supply voltage for channel 2
BOOT2	21	bootstrap high-side driver channel 2
OUT2	22	Pulse Width Modulated (PWM) output channel 2
V_{SSP2}	23	negative power supply voltage for channel 2
STAB2	24	decoupling of internal 11 V regulator for channel 2 drivers
STAB1	25	decoupling of internal 11 V regulator for channel 1 drivers
V_{SSP1}	26	negative power supply voltage for channel 1
OUT1	27	PWM output channel 1
BOOT1	28	bootstrap capacitor for channel 1
V_{DDP1}	29	positive power supply voltage for channel 1
HVP1	30	half supply output voltage 1 for charging single-ended capacitor for channel 1
OSCIO	31	oscillator input in slave configuration or oscillator output in master configuration
$V_{SSD(HW)}$	32	negative digital supply voltage and handle wafer connection

8. Functional description

8.1 General

The TDA8933 is a mono full bridge or stereo half bridge audio power amplifier using class-D technology. The audio input signal is converted into a Pulse Width Modulated (PWM) signal via an analog input stage and PWM modulator. To enable the output power Diffusion Metal Oxide Semiconductor (DMOS) transistors to be driven, this digital PWM signal is applied to control and handshake block and driver circuits for both the high side and low side. A 2nd-order-low-pass filter converts the PWM signal to an analog audio signal across the loudspeakers.

The TDA8933 contains two independent half bridges with full differential input stages. The loudspeakers can be connected in the following configurations:

- Mono full bridge: Bridge Tied Load (BTL)
- Stereo half bridge: Single-Ended (SE)

The TDA8933 contains circuits common to both channels, such as: the oscillator, all reference sources, the mode functionality and a digital timing manager.

The following protections are built-in: thermal foldback, temperature, current and voltage.

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8.2 Mode selection and interfacing

The TDA8933 can be switched to one of four operating modes using pins POWERUP and ENGAGE:

- Sleep mode: with low supply current
- Mute mode: the amplifiers are switching idle (50 % duty cycle), but the audio signal at the output is suppressed by disabling the V_I-converter input stages. The capacitors on pins HVP1 and HVP2 have been charged to half the supply voltage (asymmetrical supply only)
- Operating mode: the amplifiers are fully operational with an output signal
- Fault mode

Both pins POWERUP and ENGAGE refer to pin CGND.

Table 4 shows the different modes as a function of the voltages on the POWERUP and ENGAGE pins.

Table 4. Mode selection for the TDA8933

Mode	Pin		
	POWERUP[1]	ENGAGE[1]	DIAG
Sleep	< 0.8 V	< 0.8 V	undefined
Mute	2 V to 6 V	< 0.8 V	> 2 V
Operating	2 V to 6 V	3 V to 6 V	> 2 V
Fault	2 V to 6 V	undefined	< 0.8 V

[1] When there are symmetrical supply conditions, the voltage applied to pins POWERUP and ENGAGE must never exceed the supply voltage (V_{DDA}, V_{DDP1} or V_{DDP2}).

If the transition between Mute mode and Operating mode is controlled via a time constant, the start-up will be pop free since the DC output offset voltage is applied gradually to the output between Mute mode and Operating mode. The bias current setting of the V_I-converters is related to the voltage on pin ENGAGE.

- Mute mode: the bias current setting of the V_I-converters is zero (V_I-converters disabled).
- Operating mode: the bias current is at maximum.

The time constant required to apply the DC output offset voltage gradually between Mute mode and Operating mode can be generated by applying a decoupling capacitor on pin ENGAGE. The value of the capacitor on pin ENGAGE should be 470 nF.

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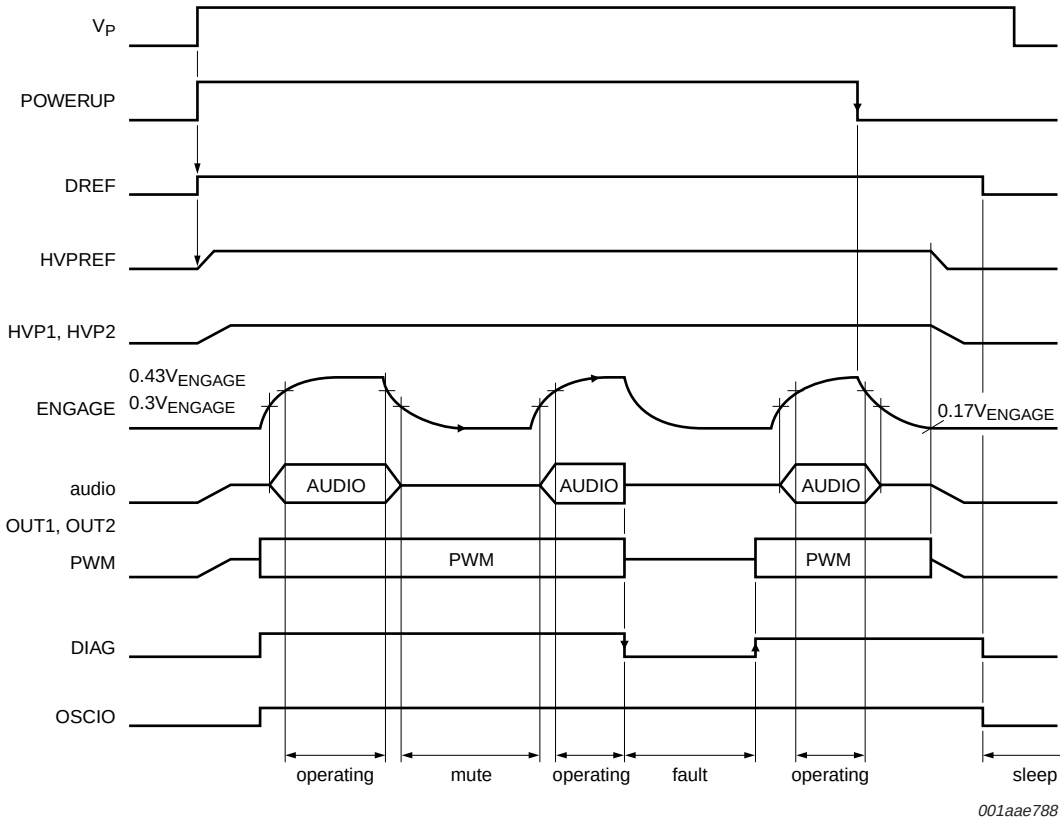


Fig 3. Start-up sequence

8.3 Pulse width modulation frequency

The output signal of the amplifier is a PWM signal with a carrier frequency of approximately 320 kHz. Using a 2nd-order-low-pass filter in the application results in an analog audio signal across the loudspeaker. The PWM switching frequency can be set by an external resistor R_{osc} connected between pin OSCREF and $V_{SSD(HW)}$. The carrier frequency can be set between 300 kHz and 500 kHz. Using an external resistor of 39 kΩ, the carrier frequency is set to an optimized value of 320 kHz (see Figure 4).

If two or more TDA8933 devices are used in the same audio application, it is recommended to synchronize the switching frequency of all devices.This can be done by connecting all the OSCIO pins together and configuring one of the TDA8933 devices in the application as the clock master. Configure the other TDA8933 devices as slaves.

Pin OSCIO is a 3-state input or output buffer. Pin OSCIO is configured in master mode as oscillator output, and in slave mode as oscillator input. Master mode is enabled by applying a resistor between pin OSCREF and $V_{SSD(HW)}$, while slave mode is enabled by connecting pin OSCREF directly to $V_{SSD(HW)}$ (without any resistor).

The value of the resistor also sets the frequency of the carrier and can be calculated with Equation 1:

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$$f_{osc} = \frac{12.45x10^{9}}{R_{osc}} \quad (1)$$

Where:

f_{osc} = oscillator frequency (Hz)

R_{osc} = oscillator resistor (Ω) (on pin OSCREF)

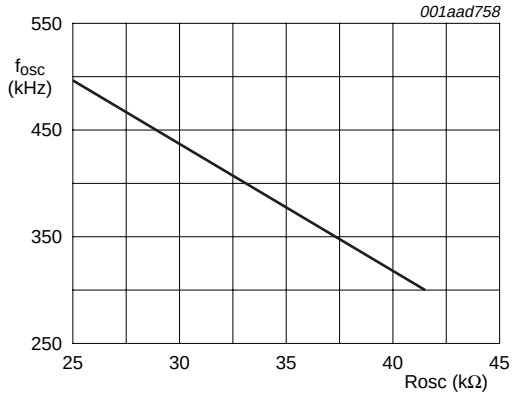


Fig 4. Oscillation frequency as a function of R_{osc}

Table 5 summarizes how to configure the TDA8933 in master or slave configuration.

Table 5. Master/slave configuration

Configuration	Pin	
	OSCREF	OSCIO
Master	R_{osc} > 25 kΩ to $V_{SSD(HW)}$	output
Slave	R_{osc} = 0 Ω; shorted to $V_{SSD(HW)}$	input

8.4 Protections

The following protections are implemented in the TDA8933:

- Thermal Foldback (TF)
- OverTemperature Protection (OTP)
- OverCurrent Protection (OCP)
- Window Protection (WP)
- Supply voltage protections
  - UnderVoltage Protection (UVP)
  - OverVoltage Protection (OVP)
  - UnBalance Protection (UBP)
- ElectroStatic Discharge (ESD)

The behavior of the device under the different fault conditions differs according to the protection activated and is described in the following sections.

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8.4.1 Thermal Foldback (TF)

If the junction temperature of the TDA8933 exceeds the threshold level (T_j > 140 °C), the gain of the amplifier is decreased gradually to a level where the combination of dissipation (P) and the thermal resistance from junction to ambient ($R_{th(j-a)}$) results in a junction temperature around the threshold level.

This means that the device will not switch off completely, but remains operational at lower output power levels. With music output signals, this feature enables high peak output powers while still operating without any external heat sink other than the printed-circuit board area.

If the junction temperature still increases due to external causes, the OverTemperature Protection (OTP) shuts down the amplifier completely.

8.4.2 OverTemperature Protection (OTP)

If the junction temperature T_j > 155 °C, the power stage will shut down immediately.

8.4.3 OverCurrent Protection (OCP)

When the output current of the device exceeds 2 A due to a short-circuit across the load or an impedance drop, the cycle-by-cycle current limitation becomes active. This means the device will not switch off, but continue to operate while limiting the current without causing audio holes (interruptions). The maximum output current will not go beyond the absolute maximum current.

If the current exceeds 2 A due to a low ohmic short from the demodulated output (after the inductor) to either V_{SS} or V_{DD} both power stages become floating. The DIAG is set low for 50 ms and the internal timer of 100 ms is started. The timer will keep both power stages disabled for 100 ms. As long as the short remains, this cycle will repeat. The average power dissipation in the TDA8933 will be low because the short-circuit current will flow only during a very small part of the timer cycle of 100 ms.

8.4.4 Window Protection (WP)

WP checks the PWM output voltage before switching from Sleep mode to Mute mode (outputs switching) and is activated:

- During the start-up sequence, when pin POWERUP is switched from Sleep mode to Mute mode.
  In the event of a short-circuit at one of the output terminals to V_{DDP1}, V_{SSP1}, V_{DDP2} or V_{SSP2} the start-up procedure is interrupted and the TDA8933 waits for open-circuit outputs. Because the check is done before enabling the power stages, no large currents will flow in the event of a short-circuit.
- When the amplifier is shut down completely, due to activation of the OCP because a short to one of the supply lines is made, then during restart (after 100 ms) the window protection will be activated. As a result, the amplifier will not start up until the short to the supply lines is removed.

8.4.5 Supply voltage protections

If the supply voltage drops below 10 V, the UVP circuit is activated and the system will shut down directly. This switch-off will be silent and without pop noise. When the supply voltage rises above the threshold level, the system is restarted again after 100 ms.

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If the supply voltage exceeds 36 V, the OVP circuit is activated and the power stages will shut down. It is re-enabled as soon as the supply voltage drops below the threshold level. The system is restarted again after 100 ms.

It should be noted that supply voltages > 40 V may damage the TDA8933. Two conditions should be distinguished:

- If the supply voltage is pumped to higher values by the TDA8933 application itself (see also Section 14.8), the OVP is triggered and the TDA8933 is shut down. The supply voltage will decrease and the TDA8933 is protected against any overstress.
- If a supply voltage > 40 V is caused by other or external causes, the TDA8933 will shut down, but the device can still be damaged since the supply voltage will remain > 40 V in this case. The OVP protection is not a supply clamp.

An additional UBP circuit compares the positive analog supply voltage (V_{DDA}) and the negative analog supply voltage (V_{SSA}) and is triggered if the voltage difference between them exceeds a certain level. This level depends on the sum of both supply voltages. The unbalance threshold levels can be defined as follows:

- LOW-level threshold: $V_{P(th)(ubp)l} < 8/5 \times V_{HVPREF}$
- HIGH-level threshold: $V_{P(th)(ubp)h} > 8/3 \times V_{HVPREF}$

In a symmetrical supply the UBP is released when the unbalance of the supply voltage is within 6 % of its starting value.

Table 6 shows an overview of all protections and the effect on the output signal.

Table 6. Overview of protections for the TDA8933

Protection	Restart	
	When fault is removed	Every 100 ms
OTP	no	yes
OCP	yes	no
WP	yes	no
UVP	no	yes
OVP	no	yes
UBP	no	yes

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8.5 Diagnostic input and output

Whenever one of the protections is triggered, except for TF, pin DIAG is activated to LOW level (see Table 6). An internal reference supply will pull up the open-drain DIAG output to approximately 2.4 V. This internal reference supply can deliver approximately 50 μA. The DIAG pin refers to pin CGND.The diagnostic output signal during different short circuit conditions is illustrated in Figure 5. Using pin DIAG as input, a voltage < 0.8 V will put the device into Fault mode.

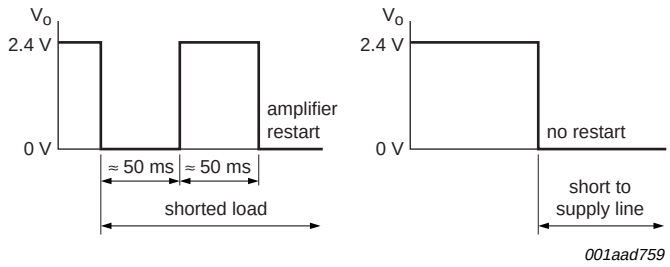


Fig 5. Diagnostic output for different kinds of short circuit conditions

8.6 Differential inputs

For a high common-mode rejection ratio and for maximum flexibility in the application, the audio inputs are fully differential. By connecting the inputs anti-parallel, the phase of one of the two channels can be inverted, so that the amplifier can operate as a mono BTL amplifier. The input configuration for a mono BTL application is illustrated in Figure 6.

In the single-ended configuration it is also recommended to connect the two differential inputs in anti-phase. This has advantages for the current handling of the power supply at low signal frequencies and minimizes supply pumping (see also Section 14.8).

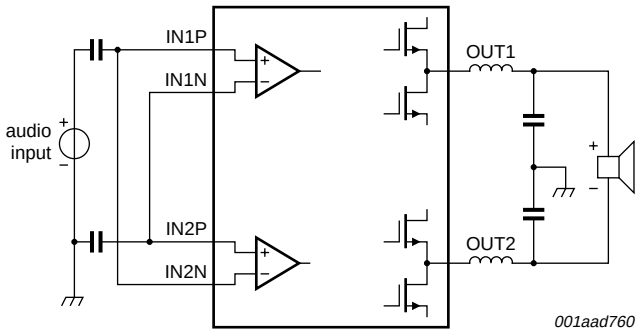


Fig 6. Input configuration for a mono BTL application

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8.7 Output voltage buffers

When pin POWERUP is set HIGH, the half supply output voltage buffers are switched on in asymmetrical supply configuration. The start-up will be pop free because the device starts switching when the capacitor on pin HVPREF and the SE capacitors are completely charged.

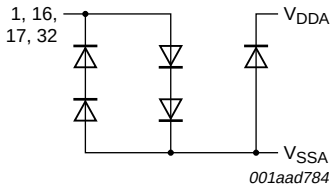
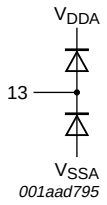
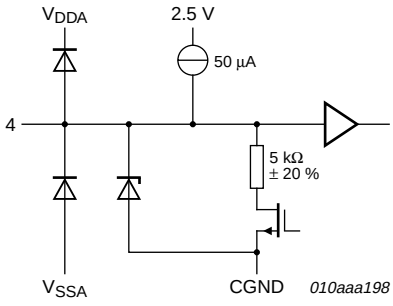
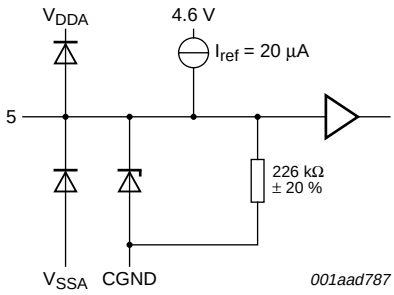
Output voltage buffers:

- Pins HVP1 and HVP2: The time required for charging the SE capacitor depends on its value. The half supply voltage output is disabled when the TDA8933 is used in a symmetrical supply application.
- Pin HVPREF: This output voltage reference buffer charges the capacitor on pin HVPREF.
- Pin INREF: This output voltage reference buffer charges the input reference capacitor on pin INREF. Pin INREF applies the bias voltage for the inputs.

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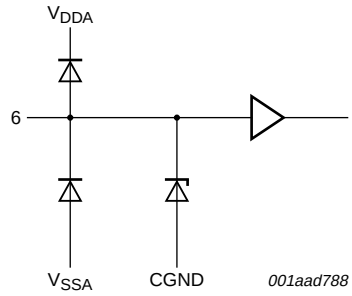
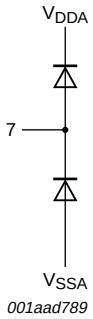
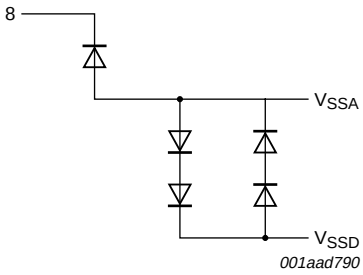
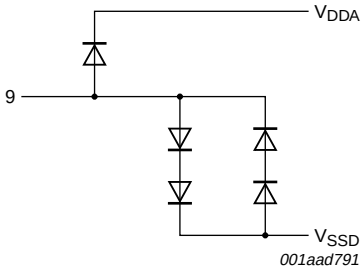
9. Internal circuitry

Table 7. Internal circuitry

Pin	Symbol	Equivalent circuit
1, 16, 17, 32	$V_{SSD(HW)}$	
2	IN1P	
3	IN1N	
12	INREF	
14	IN2N	
15	IN2P	
4	DIAG	
5	ENGAGE	

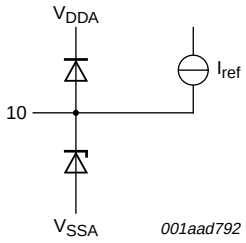
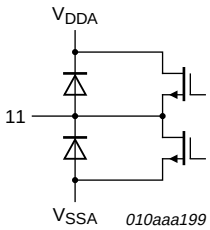
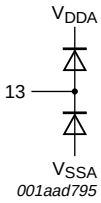
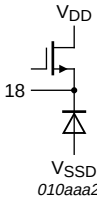
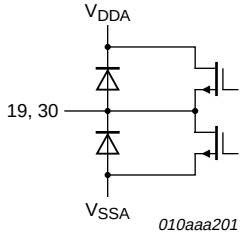
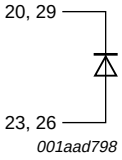
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Table 7. Internal circuitry *...continued*

Pin	Symbol	Equivalent circuit
6	POWERUP	
7	CGND	
8	V_{DDA}	
9	V_{SSA}	

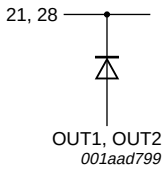
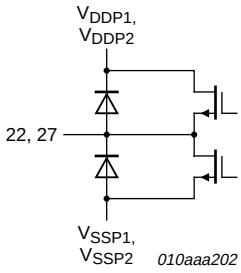
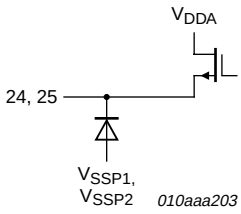
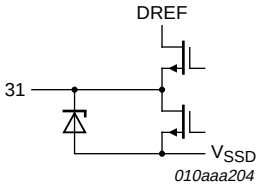
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Table 7. Internal circuitry *...continued*

Pin	Symbol	Equivalent circuit
10	OSCREF	
11	HVPREF	
13	TEST	
18	DREF	
19	HVP2	
30	HVP1	
20	V_{DDP2}	
23	V_{SSP2}	
26	V_{SSP1}	
29	V_{DDP1}	

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Table 7. Internal circuitry *...continued*

Pin	Symbol	Equivalent circuit
21	BOOT2	
28	BOOT1	
22	OUT2	
27	OUT1	
24	STAB2	
25	STAB1	
31	OSCIO	

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10. Limiting values

Table 8. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_P	supply voltage	asymmetrical supply		–0.3	+40	V
V_x	voltage on pin x					
	IN1P, IN1N, IN2P, IN2N		[1]	–5	+5	V
	OSCREF, OSCIO, TEST		[2]	$V_{SSD(HW)}$ - 0.3	5	V
	POWERUP, ENGAGE, DIAG		[3]	V_{CGND} - 0.3	6	V
	all other pins		[4]	V_{SS} - 0.3	V_{DD} + 0.3	V
I_{ORM}	repetitive peak output current	maximum output current limiting	[5]	2.3	-	A
T_j	junction temperature			-	150	°C
T_{stg}	storage temperature			–55	+150	°C
T_{amb}	ambient temperature			–40	+85	°C
P	power dissipation			-	5	W

[1] Measured with respect to pin INREF; $V_x < V_{DD} + 0.3$ V.

[2] Measured with respect to pin $V_{SSD(HW)}$; $V_x < V_{DD} + 0.3$ V.

[3] Measured with respect to pin CGND; $V_x < V_{DD} + 0.3$ V.

[4] $V_{SS} = V_{SSP1} = V_{SSP2}$; $V_{DD} = V_{DDP1} = V_{DDP2}$.

[5] Current limiting concept.

11. Thermal characteristics

Table 9. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	free air natural convection			-		
		JEDEC test board	[1]	-	41	44	K/W
		2 layer application board	[2]	-	44	-	K/W
Ψ_{j-lead}	thermal characterization parameter from junction to lead			-	-	30	K/W
Ψ_{j-top}	thermal characterization parameter from junction to top of package		[3]	-	-	8	K/W

[1] Measured in a JEDEC high K-factor test board (standard EIA/JESD 51-7) in free air with natural convection.

[2] 2 layer application board (55 mm × 45 mm), 35 μm copper, FR4 base material in free air with natural convection.

[3] Strongly dependent on where the measurement is taken on the package.

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12. Static characteristics

Table 10. Characteristics

V_P = 25 V, f_{osc} = 320 kHz and T_{amb} = 25 °C; unless specified otherwise.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply						
V_P	supply voltage	asymmetrical supply	10	25	36	V
		symmetrical supply	±5	±12.5	±18	V
I_P	supply current	Sleep mode	-	0.6	1.0	mA
$I_{q(tot)}$	total quiescent current	Operating mode; no load, no snubbers or filter connected	-	40	50	mA
Series resistance output switches						
R_{DSon}	drain-source on-state resistance	T_j = 25 °C	-	350	-	mΩ
		T_j = 125 °C	-	545	-	mΩ
Power up input: pin POWERUP[1]						
V_I	input voltage		0	-	6.0	V
I_I	input current	V_I = 3 V	-	1	20	µA
V_{IL}	LOW-level input voltage		0	-	0.8	V
V_{IH}	HIGH-level input voltage		2	-	6.0	V
Engage input: pin ENGAGE[1]						
V_O	output voltage		4.2	4.6	5.0	V
V_I	input voltage		0	-	6.0	V
I_O	output current	V_I = 3 V	-	20	40	µA
V_{IL}	LOW-level input voltage		0	-	0.8	V
V_{IH}	HIGH-level input voltage		3	-	6.0	V
Diagnostic output: pin DIAG[1]						
V_O	output voltage	protection activated; see Table 6	-	-	0.8	V
		Operating mode	2	2.5	3.3	V
Bias voltage for inputs: pin INREF						
$V_{O(bias)}$	bias output voltage	Reference to V_{SSA}	-	2.1	-	V
Half supply voltage						
Pins HVP1 and HVP2						
V_O	output voltage	half supply voltage to charge SE capacitor	$0.5V_P$ – 0.2 V	$0.5V_P$	$0.5V_P$ + 0.2 V	V
I_O	output current	$V_{HVP1} = V_{HVP2} = V_O$ – 1 V		50		mA
Pin HVPREF						
V_O	output voltage	half supply reference voltage in Mute mode	$0.5V_P$ – 0.2 V	$0.5V_P$	$0.5V_P$ + 0.2 V	V
Reference voltage for internal logic: pin DREF						
V_O	output voltage		4.5	4.8	5.1	V

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Table 10. Characteristics *...continued*

V_P = 25 V, f_{osc} = 320 kHz and T_{amb} = 25 °C; unless specified otherwise.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Amplifier outputs: pins OUT1 and OUT2						
$V_{O(offset)}$	output offset voltage	SE; with respect to HVPREF				
		Mute mode	-	-	15	mV
		Operating mode	-	-	100	mV
		BTL				
		Mute mode	-	-	20	mV
		Operating mode	-	-	150	mV
Stabilizer output: pins STAB1, STAB2						
V_O	output voltage	Mute mode and Operating mode; with respect to pins V_{SSP1} and V_{SSP2}	10	11	12	V
Voltage protections						
$V_{P(uvp)}$	undervoltage protection supply voltage		8.0	9.5	9.9	V
$V_{P(ovp)}$	overvoltage protection supply voltage		36.1	38.5	40	V
$V_{P(th)(ubp)l}$	low unbalance protection threshold supply voltage	V_{HVPREF} = 11 V	-	-	18	V
$V_{P(th)(ubp)h}$	high unbalance protection threshold supply voltage	V_{HVPREF} = 11 V	29	-	-	V
Current protections						
$I_{O(ocp)}$	overcurrent protection output current	current limiting	2.0	2.3	-	A
Temperature protection						
$T_{act(th_prot)}$	thermal protection activation temperature		155	-	160	°C
$T_{act(th_fold)}$	thermal foldback activation temperature		140	-	150	°C
Oscillator reference: pin OSCIO[2]						
V_{IH}	HIGH-level input voltage		4.0	-	5.0	V
V_{IL}	LOW-level input voltage		0	-	0.8	V
V_{OH}	HIGH-level output voltage		4.0	-	5.0	V
V_{OL}	LOW-level output voltage		0	-	0.8	V
$N_{slave(max)}$	maximum number of slaves	driven by one master	12	-	-	-

[1] Measured with respect to pin CGND.

[2] Measured with respect to pin $V_{SSD(HW)}$.

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13. Dynamic characteristics

Table 11. Switching characteristics

V_P = 25 V; T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Internal oscillator						
f_{osc}	oscillator frequency	R_{osc} = 39 kΩ	-	320	-	kHz
		range	300	-	500	kHz
Timing PWM output: pins OUT1 and OUT2						
t_r	rise time	I_O = 0 A	-	10	-	ns
t_f	fall time	I_O = 0 A	-	10	-	ns
$t_{w(min)}$	minimum pulse width	I_O = 0 A	-	80	-	ns

Table 12. SE characteristics

V_P = 25 V, R_L = 2 × 8 Ω, f_i = 1 kHz, f_{osc} = 320 kHz, R_S < 0.1 Ω [6] and T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$P_{o(RMS)}$	RMS output power	continuous time output power per channel	[1]				
		R_L = 4 Ω; V_P = 17 V					
		THD+N = 0.5 %, f_i = 1 kHz		5.9	6.5	-	W
		THD+N = 0.5 %, f_i = 100 Hz		-	6.5	-	W
		THD+N = 10 %, f_i = 1 kHz		7.5	8.3	-	W
		THD+N = 10 %, f_i = 100 Hz		-	8.3	-	W
		R_L = 8 Ω; V_P = 25 V					
		THD+N = 0.5 %, f_i = 1 kHz		7.3	8.1	-	W
		THD+N = 0.5 %, f_i = 100 Hz		-	8.1	-	W
		THD+N = 10 %, f_i = 1 kHz		9.3	10.3	-	W
		THD+N = 10 %, f_i = 100 Hz		-	10.3	-	W
		short time output power per channel; THD+N = 10 %, see Figure 23 for details	[2]				
		R_L = 8 Ω; V_P = 31 V					
		THD+N = 0.5 %		11.2	12.4	-	W
		THD+N = 10 %		14.1	15.7	-	W
THD+N	total harmonic distortion-plus-noise	P_o = 1 W	[3]				
		f_i = 1 kHz		-	0.011	0.1	%
		f_i = 6 kHz		-	0.06	0.1	%
$G_{v(cl)}$	closed-loop voltage gain	V_i =100 mV; no load		29	30	31	dB
$\|\Delta G_v\|$	voltage gain difference			-	0.5	1	dB
α_{cs}	channel separation	P_o = 1 W; f_i = 1 kHz		70	80	-	dB
SVRR	supply voltage ripple rejection	Operating mode	[4]				
		f_i = 100 Hz		-	60	-	dB
		f_i = 1 kHz		40	50	-	dB
$\|Z_i\|$	input impedance	differential		70	100	-	kΩ

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Table 12. SE characteristics *...continued*

V_P = 25 V, R_L = 2 × 8 Ω, f_i = 1 kHz, f_{osc} = 320 kHz, R_S < 0.1 Ω [6] and T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{n(o)}$	noise output voltage	Operating mode; R_s = 0 Ω	[5]	-	100	150	μV
		Mute mode	[5]	-	70	100	μV
$V_{O(mute)}$	mute output voltage	Mute mode; V_i = 1 V (RMS) and f_i = 1 kHz		-	100	-	μV
CMRR	common mode rejection ratio	$V_{i(cm)}$ = 1 V (RMS)		-	75	-	dB
η_{po}	output power efficiency	P_o = 10 W					
		V_P = 17 V; R_L = 4 Ω		86	87	-	%
		V_P = 25 V; R_L = 8 Ω		89	90	-	%

[1] Output power is measured indirectly; based on R_{DSon} measurement.

[2] 2 layer application board (55 mm × 45 mm), 35 μm copper, FR4 base material in free air with natural convection.

[3] THD+N is measured in a bandwidth of 20 Hz to 20 kHz, AES17 brick wall.

[4] Maximum V_{ripple} = 2 V (p-p); R_S = 0 Ω.

[5] B = 20 Hz to 20 kHz, AES17 brick wall.

[6] R_S is the series resistance of inductor and capacitor of low-pass LC filter in the application.

Table 13. BTL characteristics

V_P = 25 V, R_L = 16 Ω, f_i = 1 kHz, f_{osc} = 320 kHz, R_S < 0.1 Ω [5] and T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$P_{o(RMS)}$	RMS output power	continuous time output power: THD+N = 10 %; f_i = 1 kHz	[1]				
		R_L = 8 Ω; V_P = 17 V					
		THD+N = 0.5 %, f_i = 1 kHz		11.9	13.2	-	W
		THD+N = 0.5 %, f_i = 100 Hz		-	13.2	-	W
		THD+N = 10 %, f_i = 1 kHz		15.4	17.1	-	W
		THD+N = 10 %, f_i = 100 Hz		-	17.1	-	W
		R_L = 16 Ω; V_P = 25 V					
		THD+N = 0.5 %, f_i = 1 kHz		14.9	16.5	-	W
		THD+N = 0.5 %, f_i = 100 Hz		-	16.5	-	W
		THD+N = 10 %, f_i = 1 kHz		18.9	21	-	W
		THD+N = 10 %, f_i = 100 Hz		-	21	-	W
		short time output power; THD+N = 10 %, see Figure 35 for details	[2]				
		R_L = 16 Ω; V_P = 31 V					
		THD+N = 0.5 %		22.8	25.3	-	W
		THD+N = 10 %		28.8	32	-	W
THD+N	total harmonic distortion-plus-noise	P_o = 1 W	[3]				
		f_i = 1 kHz		-	0.04	0.1	%
		f_i = 10 kHz		-	0.18	0.24	%
$G_{v(cl)}$	closed-loop voltage gain			35	36	37	dB
$\|Z_i\|$	input impedance	differential		35	50	-	kΩ

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Table 13. BTL characteristics *…continued*

V_P = 25 V, R_L = 16 Ω, f_i = 1 kHz, f_{osc} = 320 kHz, R_S < 0.1 Ω [5] and T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{n(o)}$	noise output voltage	R_S = 0 Ω					
		Operating mode	[4]	-	100	150	μV
		Mute mode	[4]	-	70	100	μV
$V_{O(mute)}$	mute output voltage	Mute mode; V_i = 1 V (RMS) and f_i = 1 kHz		-	100	-	μV
CMRR	common mode rejection ratio	$V_{i(cm)}$ = 1 V (RMS)		-	75	-	dB
η_{po}	output power efficiency	P_o = 17 W; V_P = 17 V; R_L = 8 Ω		87	89	-	%
		P_o = 21 W; V_P = 25 V; R_L = 16 Ω		90	92	-	%

[1] Output power is measured indirectly; based on R_{DSon} measurement.

[2] 2 layer application board (55 mm × 45 mm), 35 μm copper, FR4 base material in free air with natural convection.

[3] THD+N is measured in a bandwidth of 20 Hz to 20 kHz, AES17 brick wall.

[4] B = 22 Hz to 20 kHz, AES17 brick wall.

[5] R_S is the series resistance of inductor and capacitor of low-pass LC filter in the application.

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14. Application information

14.1 Output power estimation

The output power P_o at THD+N = 0.5 %, just before clipping, for the SE and BTL configurations can be estimated using Equation 2 and Equation 3.

SE configuration:

$$P_{o(0.5\ \%)} = \frac{\left[\left(\frac{R_L}{R_L + R_{DSon} + R_s + R_{ESR}}\right) \times (1 - t_{w(min)} \times f_{osc}) \times V_P\right]^2}{8 \times R_L} \quad (2)$$

BTL configuration:

$$P_{o(0.5\ \%)} = \frac{\left[\left(\frac{R_L}{R_L + 2 \times (R_{DSon} + R_s)}\right) \times (1 - t_{w(min)} \times f_{osc}) \times V_P\right]^2}{2 \times R_L} \quad (3)$$

Where:

V_P = supply voltage V_{DDP1} - V_{SSP1} (V) or V_{DDP2} - V_{SSP2} (V)

R_L = load resistance (Ω)

R_{DSon} = drain-source on-state resistance (Ω)

R_s = series resistance output inductor (Ω)

R_{ESR} = equivalent series resistance SE capacitance (Ω)

$t_{w(min)}$ = minimum pulse width (s); 80 ns typical

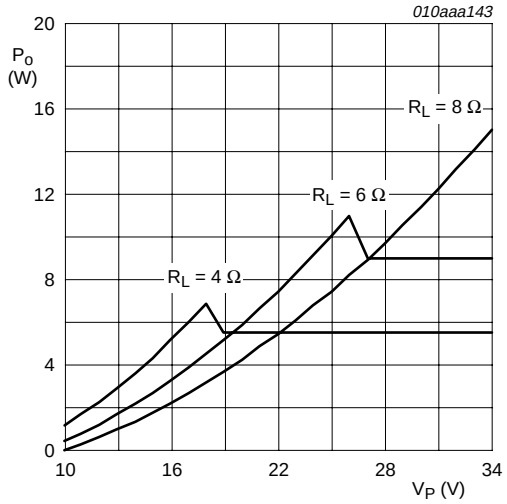
f_{osc} = oscillator frequency (Hz); 320 kHz typical with R_{osc} = 39 kΩ

The output power P_o at THD+N = 10 % can be estimated by:

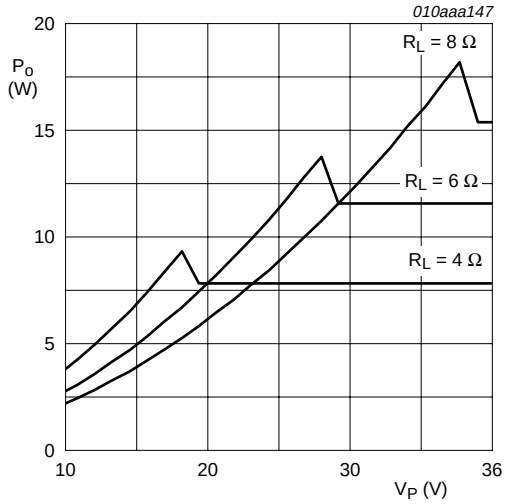
$$P_{o(10\ \%)} = 1.25 \times P_{o(0.5\ \%)} \quad (4)$$

Figure 7 and Figure 8 show the estimated output power at THD+N = 0.5 % and THD+N = 10 % as a function of the supply voltage for SE and BTL configurations at different load impedances. The output power is calculated with: R_{DSon} = 0.35 Ω (at T_j = 25 °C), R_s = 0.05 Ω, R_{ESR} = 0.05 Ω and $I_{O(ocp)}$ = 2 A (minimum).

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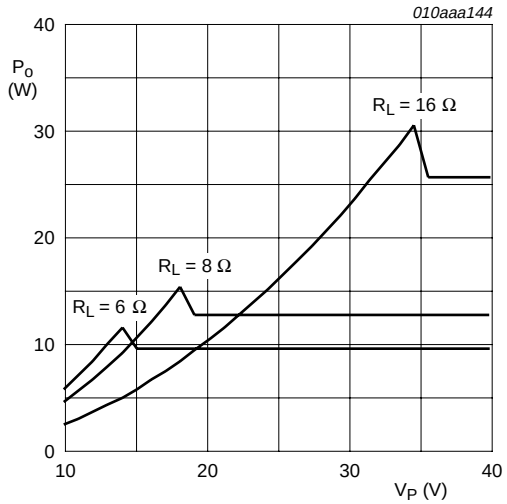
a. THD+N = 0.5 %



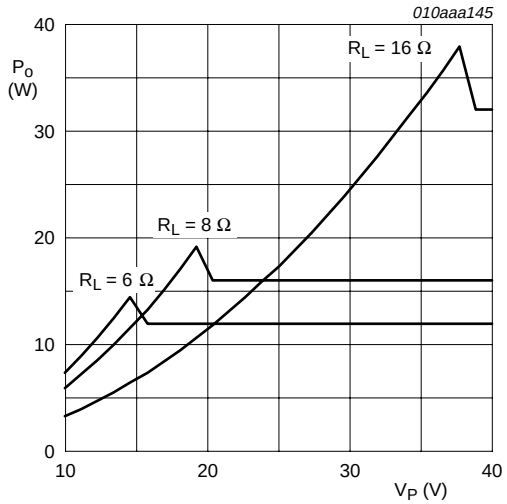
b. THD+N = 10 %

(1) When the maximum current of 2 A is reached, the current limitation feature becomes active. See also Section 8.4.3 for OCP details.

Fig 7. SE output power as a function of supply voltage



a. THD+N = 0.5 %



b. THD+N = 10 %

(1) When the maximum current of 2 A is reached, the current limitation feature becomes active. See also Section 8.4.3 for OCP details.

Fig 8. BTL output power as a function of supply voltage

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14.2 Output current limiting

The peak output current I_{OM} is internally limited to 2 A (minimum). During normal operation the output current should not exceed this threshold level, otherwise the signal is distorted. The peak output current in SE or BTL configurations can be calculated using Equation 5 and Equation 6.

SE configuration:

$$I_{O(max)} \leq \frac{0.5 \times V_P}{R_L + R_{DSon} + R_s + R_{ESR}} \leq 2\ A \quad (5)$$

BTL configuration:

$$I_{O(max)} \leq \frac{V_P}{R_L + 2 \times (R_{DSon} + R_s)} \leq 2\ A \quad (6)$$

Where:

V_P = supply voltage V_{DDP1} - V_{SSP1} (V) or V_{DDP2} - V_{SSP2} (V)

R_L = load resistance (Ω)

R_{DSon} = drain-source on-state resistance (Ω)

R_s = series resistance (Ω)

R_{ESR} = equivalent series resistance SE capacitance (Ω)

Example:

An 8 Ω speaker in the BTL configuration can be used up to a supply voltage of 18 V without running into current limiting. Current limiting (clipping) will avoid audio holes but produces a similar distortion to voltage clipping.

14.3 Speaker configuration and impedance

For a flat frequency response (second order Butterworth filter) it is necessary to change the low-pass filter components L_{LC} and C_{LC} according to the speaker configuration and impedance. Table 14 shows the required values in practice.

Table 14. Filter component values

Configuration	R_L (Ω)	L_{LC} (μH)	C_{LC} (nF)
SE	4	22	680
	6	33	470
	8	47	330
BTL	8	22	680
	16	47	330

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14.4 Single-ended capacitor

The SE capacitor forms a high-pass filter with the speaker impedance. So the frequency response will roll off with 20 dB per decade below f_{-3dB} (3 dB cut-off frequency).

The 3 dB cut-off frequency is equal to:

$$f_{-3dB} = \frac{1}{2\pi \times R_L \times C_{SE}} \quad (7)$$

Where:

f_{-3dB} = 3 dB cut-off frequency (Hz)

R_L = load resistance (Ω)

C_{SE} = single-ended capacitance (F); see Figure 37.

Table 15 shows an overview of the required SE capacitor values in the case of 60 Hz, 40 Hz or 20 Hz 3 dB cut-off frequency.

Table 15. SE capacitor values

Impedance (Ω)	C_{SE} (μF)		
	f_{-3dB} = 60 Hz	f_{-3dB} = 40 Hz	f_{-3dB} = 20 Hz
4	680	1000	2200
6	470	680	1500
8	330	470	1000

14.5 Gain reduction

The gain of the TDA8933 is internally fixed at 30 dB for SE, and 36 dB for BTL. The gain can be reduced by a resistive voltage divider at the input (see Figure 9).

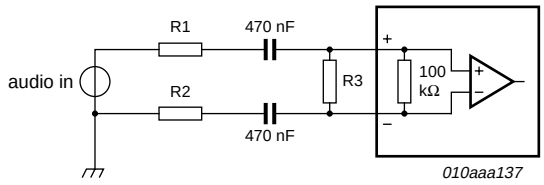


Fig 9. Input configuration for reducing gain

When applying a resistive divider, the total voltage gain $G_{v(tot)}$ can be calculated using Equation 8 and Equation 9:

$$G_{v(tot)} = G_{v(cl)} + 20log\left[\frac{R_{EQ}}{R_{EQ} + (R1 + R2)}\right] \quad (8)$$

Where:

$G_{v(tot)}$ = total voltage gain (dB)

$G_{v(cl)}$ = closed-loop voltage gain, fixed at 30 dB for SE (dB)

R_{EQ} = equivalent resistance, R3 and Z_i (Ω)

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R1 = series resistors (Ω)

R2 = series resistors (Ω)

$$R_{EQ} = \frac{R3 \times Z_i}{R3 + Z_i} \quad (9)$$

Where:

R_{EQ} = equivalent resistance (Ω)

R3 = parallel resistor (Ω)

Z_i = internal input impedance (Ω)

Example:

Substituting R1 = R2 = 4.7 kΩ, Z_i = 100 kΩ and R3 = 22 kΩ in Equation 8 and Equation 9 results in a gain of $G_{v(tot)}$ = 26.3 dB.

14.6 Device synchronization

If two or more TDA8933 devices are used in one application it is recommended that all devices are synchronized at the same switching frequency to avoid beat tones. Synchronization can be realized by connecting all OSCIO pins together and configuring one of the TDA8933 devices as master, while the other TDA8933 devices are configured as slaves (see Figure 10).

A device is configured as master when a resistor R_{osc} is connected between pin OSCREF and pin $V_{SSD(HW)}$, setting the carrier frequency. Pin OSCIO of the master is then configured as an oscillator output for synchronization. The OSCREF pins of the slave devices should be shorted to pin $V_{SSD(HW)}$, configuring pin OSCIO as an input.

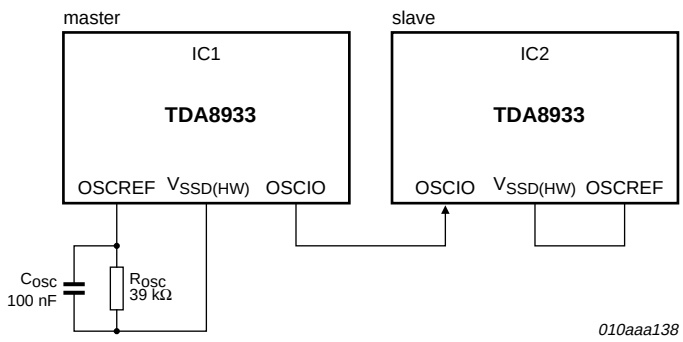


Fig 10. Master/slave concept in two-chip application

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14.7 Thermal behavior (printed-circuit board considerations)

The heat sink in an application with a TDA8933 is made using the copper on the printed-circuit board. The TDA8933 uses the four corner leads (pins 1, 16, 17 and 32) for heat transfer from the die to the PCB. The thermal foldback will limit the maximum junction temperature to 140 °C.

Equation 10 shows the relation between the maximum allowable power dissipation P and the thermal resistance from junction to ambient.

$$R_{th(j-a)} = \frac{T_{j(max)} - T_{amb}}{P} \quad (10)$$

Where:

$R_{th(j-a)}$ = thermal resistance from junction to ambient (K/W)

$T_{j(max)}$ = maximum junction temperature (°C)

T_{amb} = ambient temperature (°C)

P = power dissipation (W), which is determined by the efficiency of the TDA8933

The power dissipation is shown in Figure 21 (SE) and Figure 33 (BTL).

The thermal resistance, $R_{th(j-a)}$, of a 2 layer application board (55 mm × 45 mm), 35 µm copper, FR4 base material in free air with natural convection, is 44 K/W (typ.).

14.8 Pumping effects

When the amplifier is used in an SE configuration, a so-called 'pumping effect' can occur. During one switching interval, energy is taken from one supply (e.g. V_{DDP1}), while a part of that energy is delivered back to the other supply line (e.g. V_{SSP1}), and vice versa. When the power supply cannot sink energy, the voltage across the output capacitors of that power supply will increase.

The voltage increase caused by the pumping effect depends on:

- Speaker impedance
- Supply voltage
- Audio signal frequency
- Value of decoupling capacitors on supply lines
- Source and sink currents of other channels

The pumping effect should not cause a malfunction of either the audio amplifier or the power supply. For instance, this malfunction can be caused by triggering of the undervoltage or overvoltage protection of the amplifier.

Pumping effects in an SE configuration can be minimized by connecting audio inputs in anti-phase and changing the polarity of one speaker, as shown in Figure 11.

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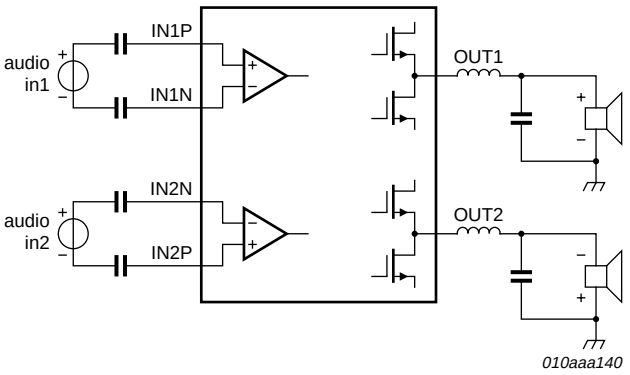
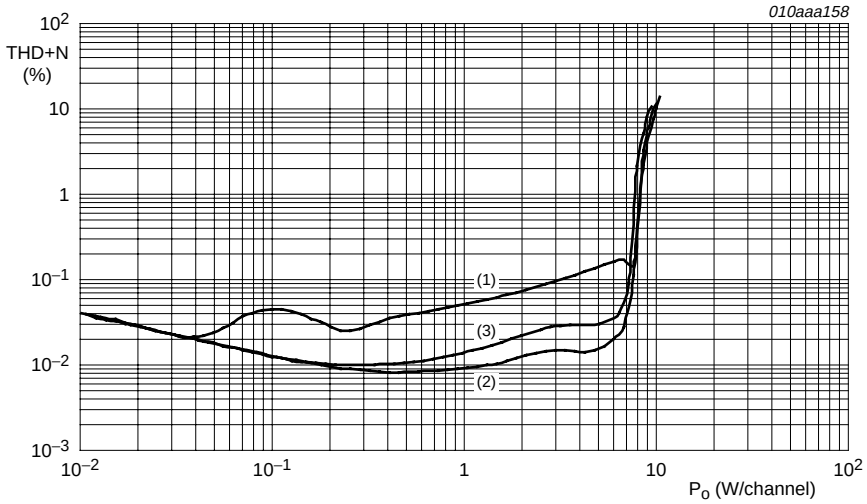


Fig 11. SE application for reducing pumping effect

14.9 SE curves measured in the reference design



(1) f_i = 6 kHz

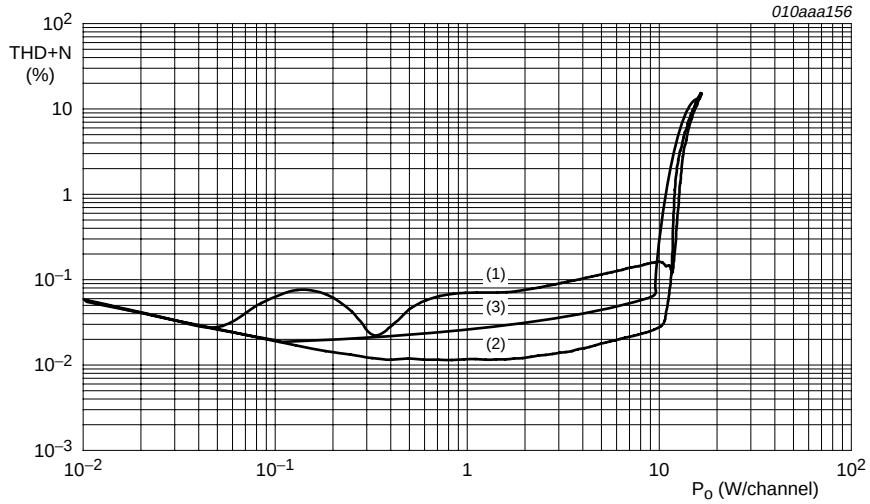
(2) f_i = 1 kHz

(3) f_i = 100 Hz

a. V_P = 25 V; R_L = 2 × 8 Ω

Fig 12. Total harmonic distortion-plus-noise as a function of output power

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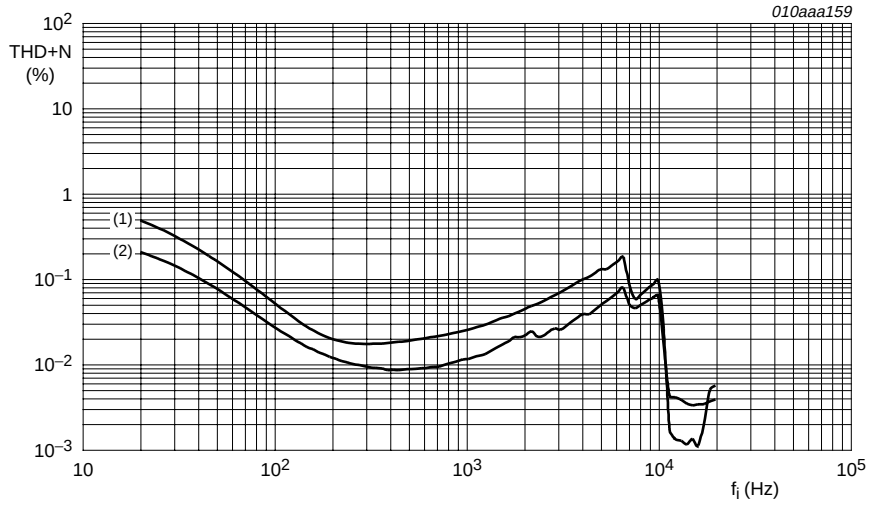
(1) f_i = 6 kHz

(2) f_i = 1 kHz

(3) f_i = 100 Hz

a. V_P = 17 V; R_L = 2 × 4 Ω

Fig 13. Total harmonic distortion-plus-noise as a function of output power



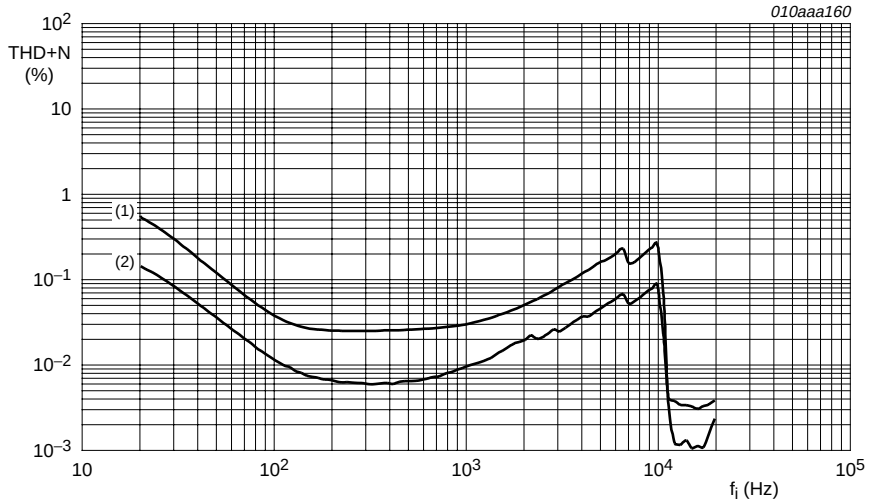
(1) P_o = 7 W

(2) P_o = 1 W

a. V_P = 25 V; R_L = 2 × 8 Ω

Fig 14. Total harmonic distortion-plus-noise as a function of frequency

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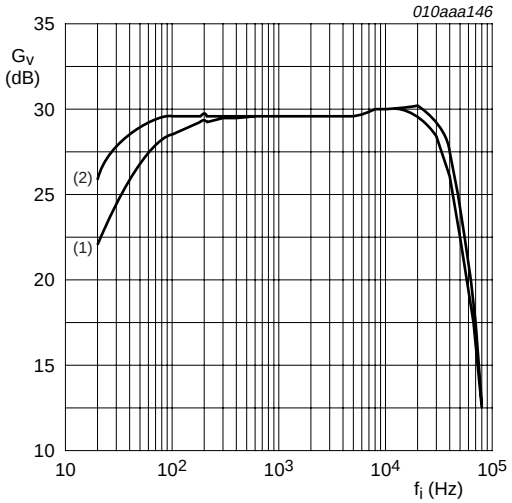


(1) P_o = 5 W

(2) P_o = 1 W

a. V_P = 17 V; R_L = 2 × 4 Ω

Fig 15. Total harmonic distortion-plus-noise as a function of frequency

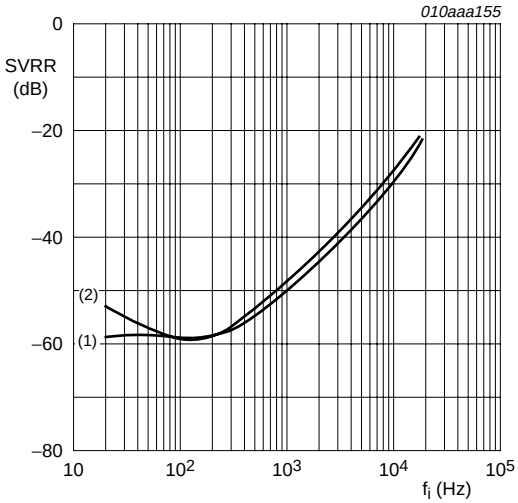


P_o = 1 W (RMS)

(1) V_P = 17 V; R_L = 2 × 4 Ω; C_{SE} = 1000 µF

(2) V_P = 25 V; R_L = 2 × 8 Ω; C_{SE} = 1000 µF

Fig 16. Gain as a function of frequency



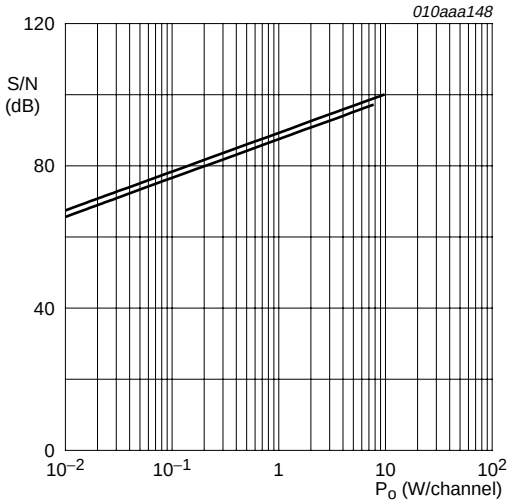
V_{ripple} = 500 mV (RMS) referenced to ground;
R_i = 0 Ω (shorted input)

(1) V_P = 17 V; R_L = 2 × 4 Ω

(2) V_P = 25 V; R_L = 2 × 8 Ω

Fig 17. Supply voltage ripple rejection as a function of frequency

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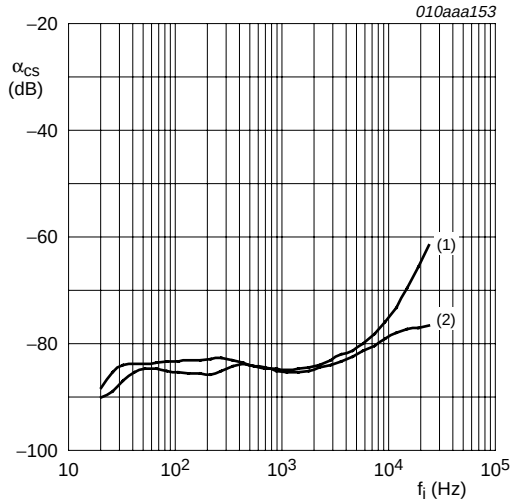


R_i = 0 Ω; 20 kHz brick wall filter AES17

(1) R_L = 2 × 4 Ω; V_P = 17 V

(2) R_L = 2 × 8 Ω; V_P = 25 V

Fig 18. Signal-to-noise ratio as a function of output power

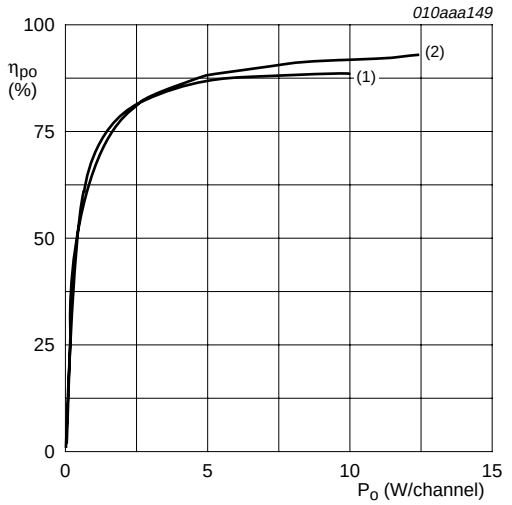


P_o = 1 W; C_{HVPREF} = 47 µF

(1) V_P = 17 V; R_L = 2 × 4 Ω

(2) V_P = 25 V; R_L = 2 × 8 Ω

Fig 19. Channel separation as a function of frequency

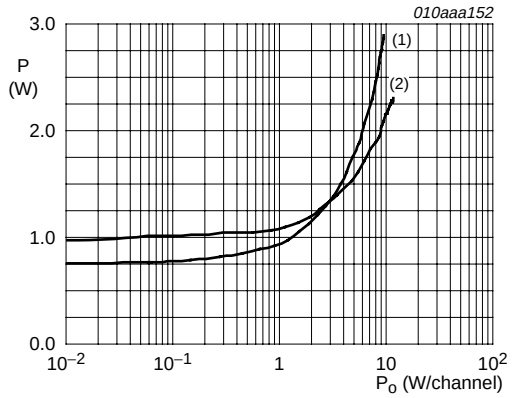


$\eta_{po} = (2 \times P_o) / (2 \times P_o + P)$

(1) V_P = 17 V; R_L = 2 × 4 Ω; f_i = 1 kHz

(2) V_P = 25 V; R_L = 2 × 8 Ω; f_i = 1 kHz

Fig 20. Output power efficiency as a function of output power



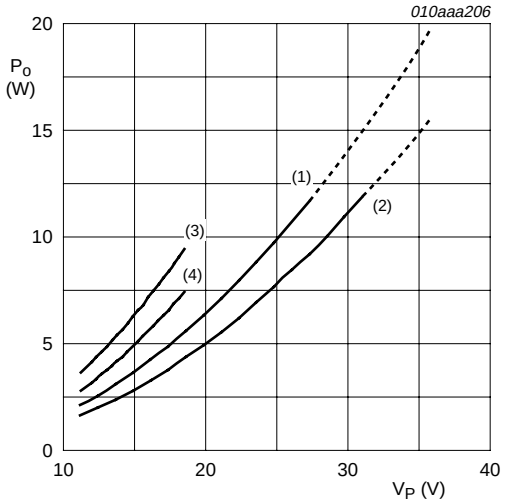
Power dissipation in junction only.

(1) V_P = 17 V; R_L = 2 × 4 Ω; f_i = 1 kHz

(2) V_P = 25 V; R_L = 2 × 8 Ω; f_i = 1 kHz

Fig 21. Power dissipation as a function of output power per channel (two channels driven)

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f_i = 1 kHz

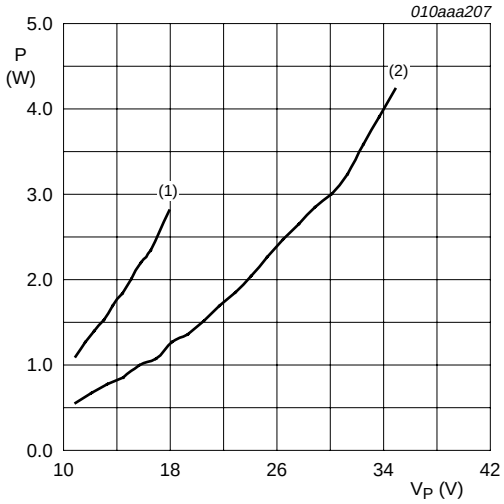
(1) $R_L = 2 \times 8\ \Omega$ SE; THD = 10 %

(2) $R_L = 2 \times 8\ \Omega$ SE; THD = 0.5 %

(3) $R_L = 2 \times 4\ \Omega$ SE; THD = 10 %

(4) $R_L = 2 \times 4\ \Omega$ SE; THD = 0.5 %

Fig 22. Output power per channel as a function of supply voltage

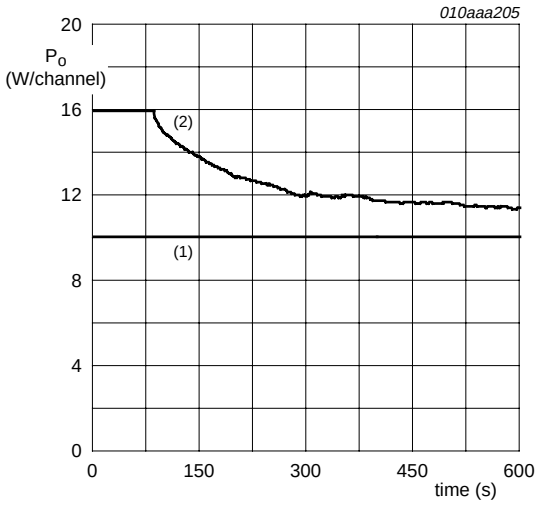


f_i = 1 kHz; power dissipation in junction only; short time P_O at THD+N = 10 %

(1) $R_L = 2 \times 4\ \Omega$ SE

(2) $R_L = 2 \times 8\ \Omega$ SE

Fig 23. Power dissipation as a function of supply voltage

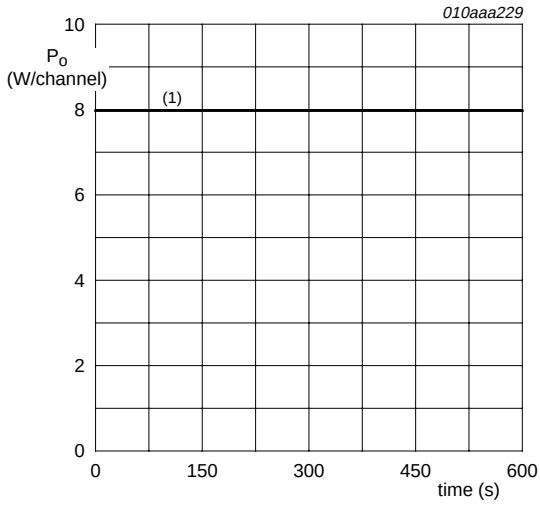


(1) V_P = 25 V

(2) V_P = 31 V

2 layer application board (55 mm × 45 mm), 35 µ copper, FR4 base material in free air with natural convection.

a. $R_L = 2 \times 8\ \Omega$ SE; f_i = 1 kHz

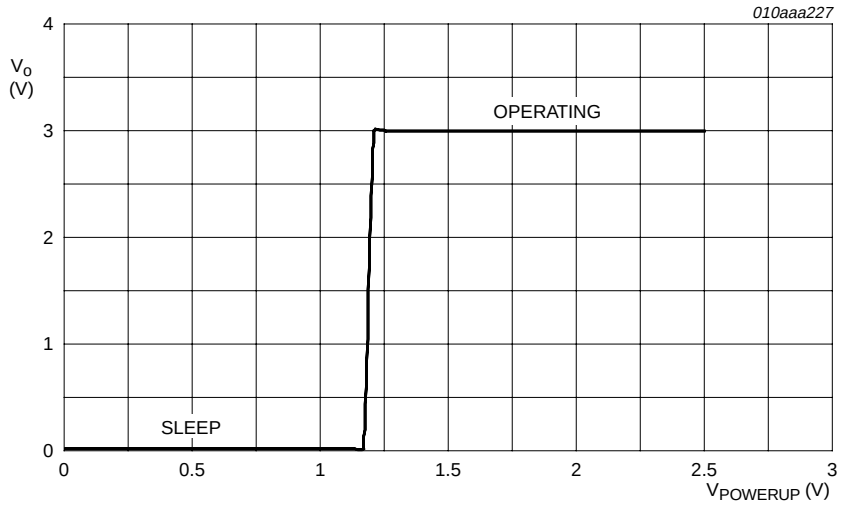


(1) V_P = 17 V

b. $R_L = 2 \times 4\ \Omega$ SE; f_i = 1 kHz

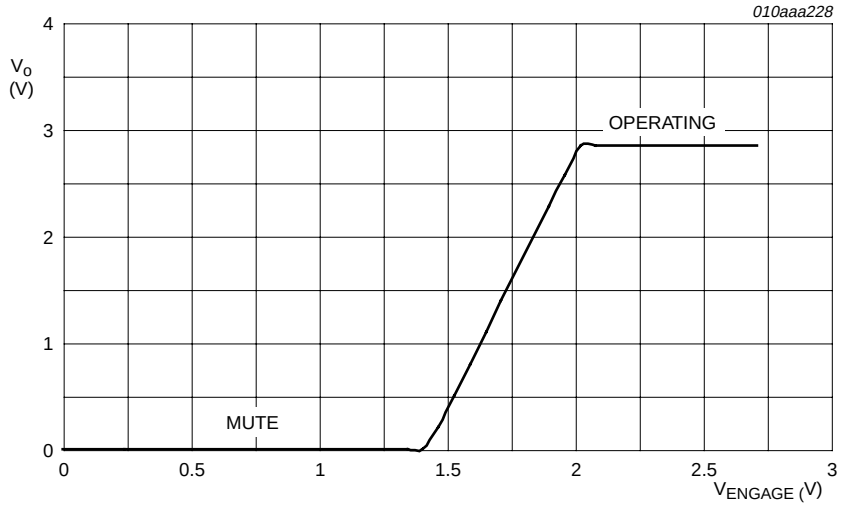
Fig 24. Output power as a function of time

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f_i = 1 kHz; V_i = 100 mV; V_{ENGAGE} > 3 V

Fig 25. Output voltage as a function of voltage on pin POWERUP

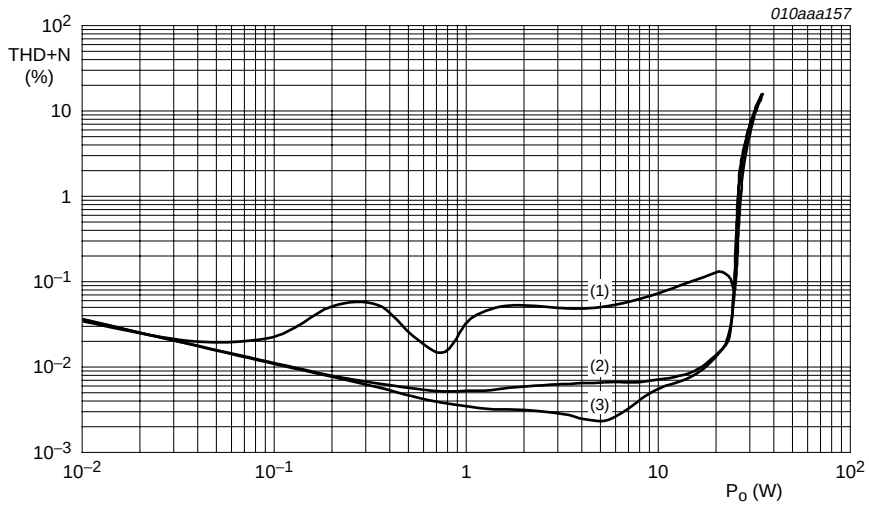


f_i = 1 kHz; V_i = 100 mV

Fig 26. Output voltage as a function of voltage on pin ENGAGE

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14.10 BTL curves measured in the reference design



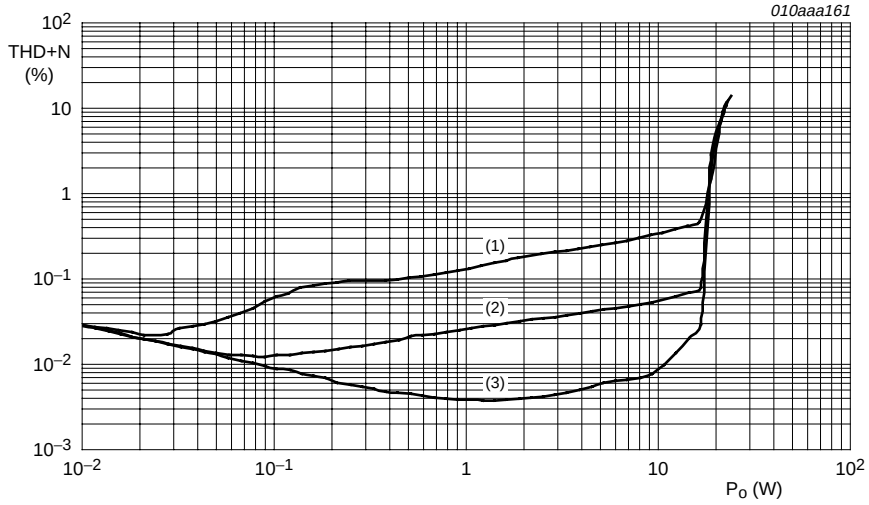
(1) f_i = 6 kHz

(2) f_i = 1 kHz

(3) f_i = 100 Hz

a. V_P = 17 V; R_L = 8 Ω

Fig 27. Total harmonic distortion-plus-noise as a function of output power



(1) f_i = 6 kHz

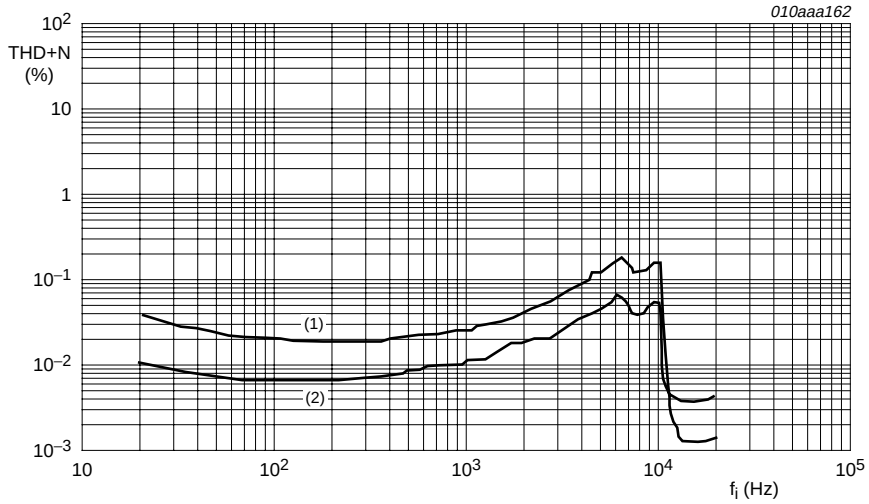
(2) f_i = 1 kHz

(3) f_i = 100 Hz

a. V_P = 25 V; R_L = 16 Ω

Fig 28. Total harmonic distortion-plus-noise as a function of output power

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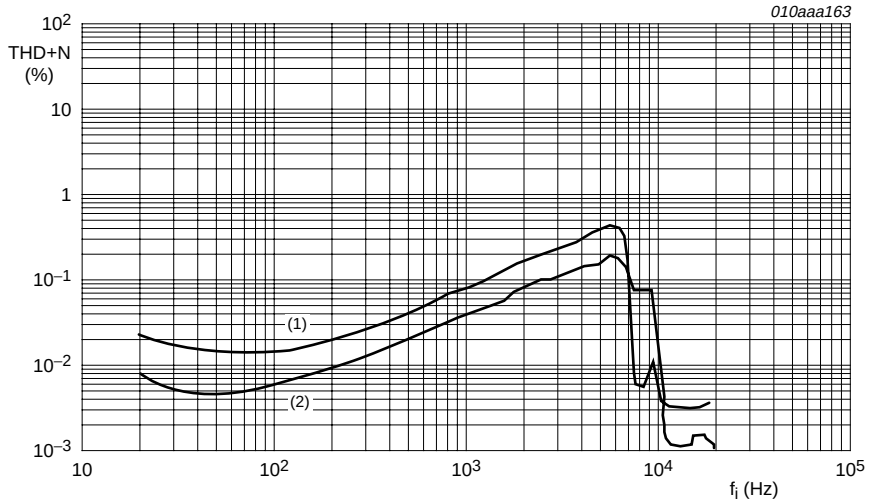


(1) P_o = 10 W

(2) P_o = 1 W

a. V_P = 17 V; R_L = 8 Ω

Fig 29. Total harmonic distortion-plus-noise as a function of frequency



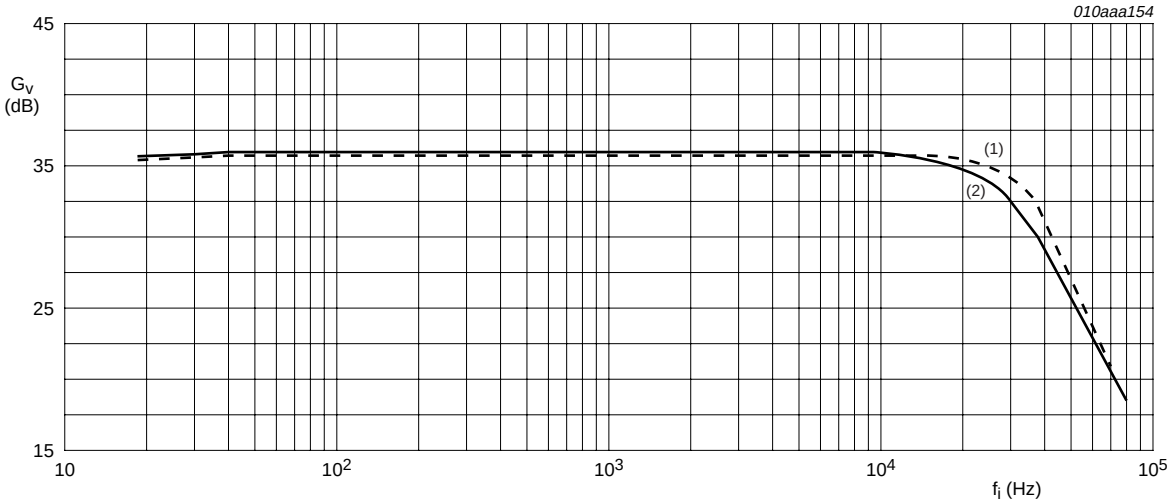
(1) P_o = 10 W

(2) P_o = 1 W

a. V_P = 25 V; R_L = 16 Ω

Fig 30. Total harmonic distortion-plus-noise as a function of frequency

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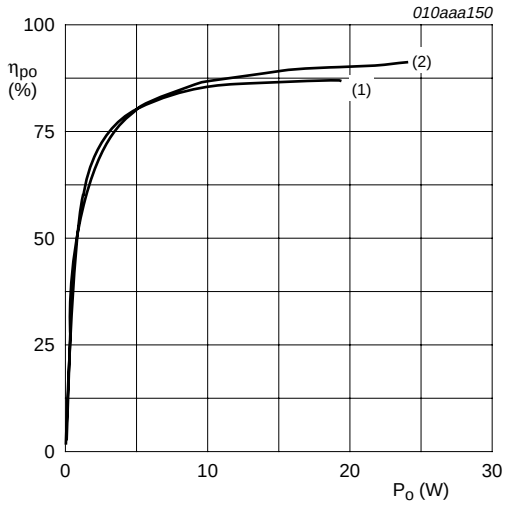


P_o = 1 W (RMS)

(1) V_P = 17 V; R_L = 8 Ω

(2) V_P = 25 V; R_L = 16 Ω

Fig 31. Gain as a function of frequency

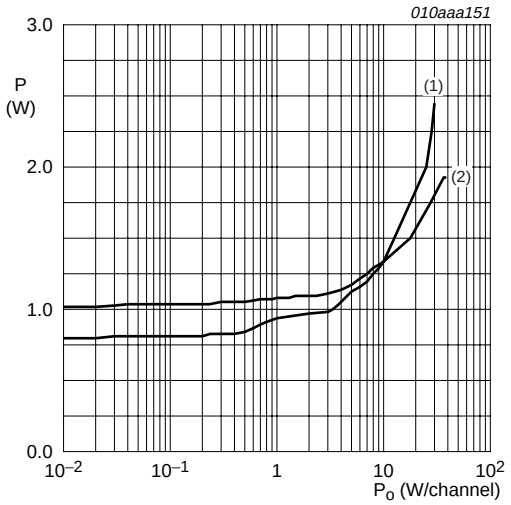


$\eta_{po} = P_o / (P_o + P)$

(1) V_P = 17 V; R_L = 8 Ω; f_i = 1 kHz

(2) V_P = 25 V; R_L = 16 Ω; f_i = 1 kHz

Fig 32. Output power efficiency as a function of output power



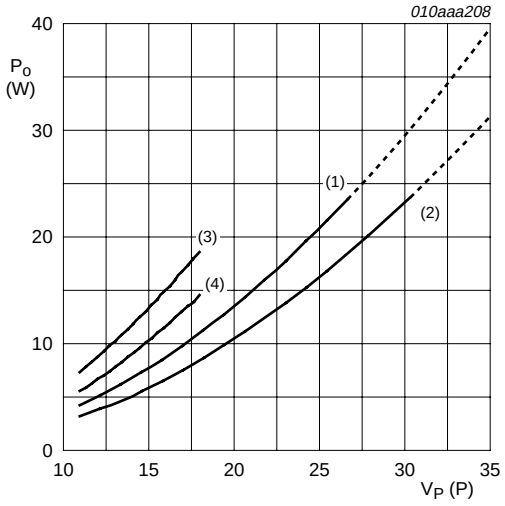
Power dissipation in junction only.

(1) V_P = 17 V; R_L = 8 Ω; f_i = 1 kHz

(2) V_P = 25 V; R_L = 16 Ω; f_i = 1 kHz

Fig 33. Power dissipation as a function of output power

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f_i = 1 kHz

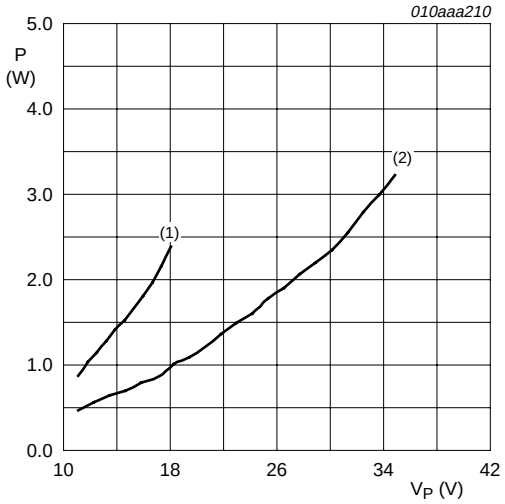
(1) R_L = 16 Ω BTL; THD = 10 %

(2) R_L = 16 Ω BTL; THD = 0.5 %

(3) R_L = 8 Ω BTL; THD = 10 %

(4) R_L = 8 Ω BTL; THD = 0.5 %

Fig 34. Output power as a function of supply voltage

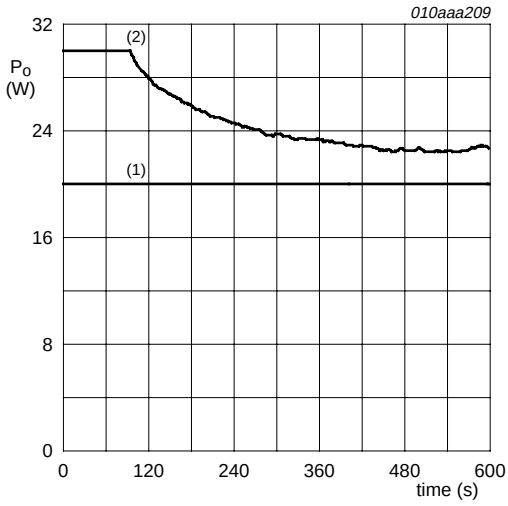


f_i = 1 kHz; power dissipation in junction only; short time P_O at THD+N = 10 %

(1) R_L = 8 Ω BTL

(2) R_L = 16 Ω BTL

Fig 35. Power dissipation as a function of supply voltage

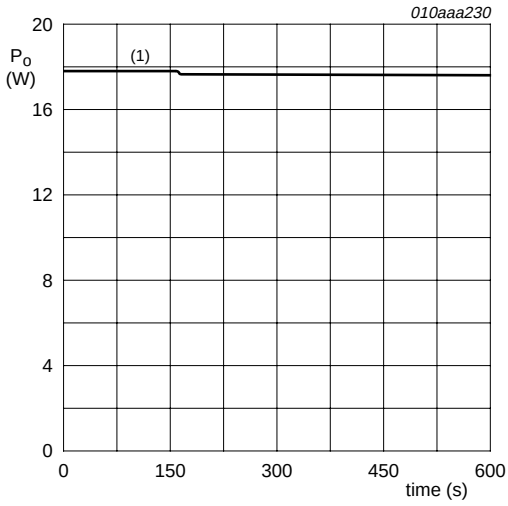


(1) V_P = 25 V

(2) V_P = 31 V

2 layer application board (55 mm × 45 mm), 35 µ copper, FR4 base material in free air with natural convection.

a. R_L = 16 Ω BTL; f_i = 1 kHz



(1) V_P = 17 V

b. R_L = 8 Ω BTL; f_i = 1 kHz

Fig 36. Output power as a function of time

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14.11 Typical application schematics (simplified)

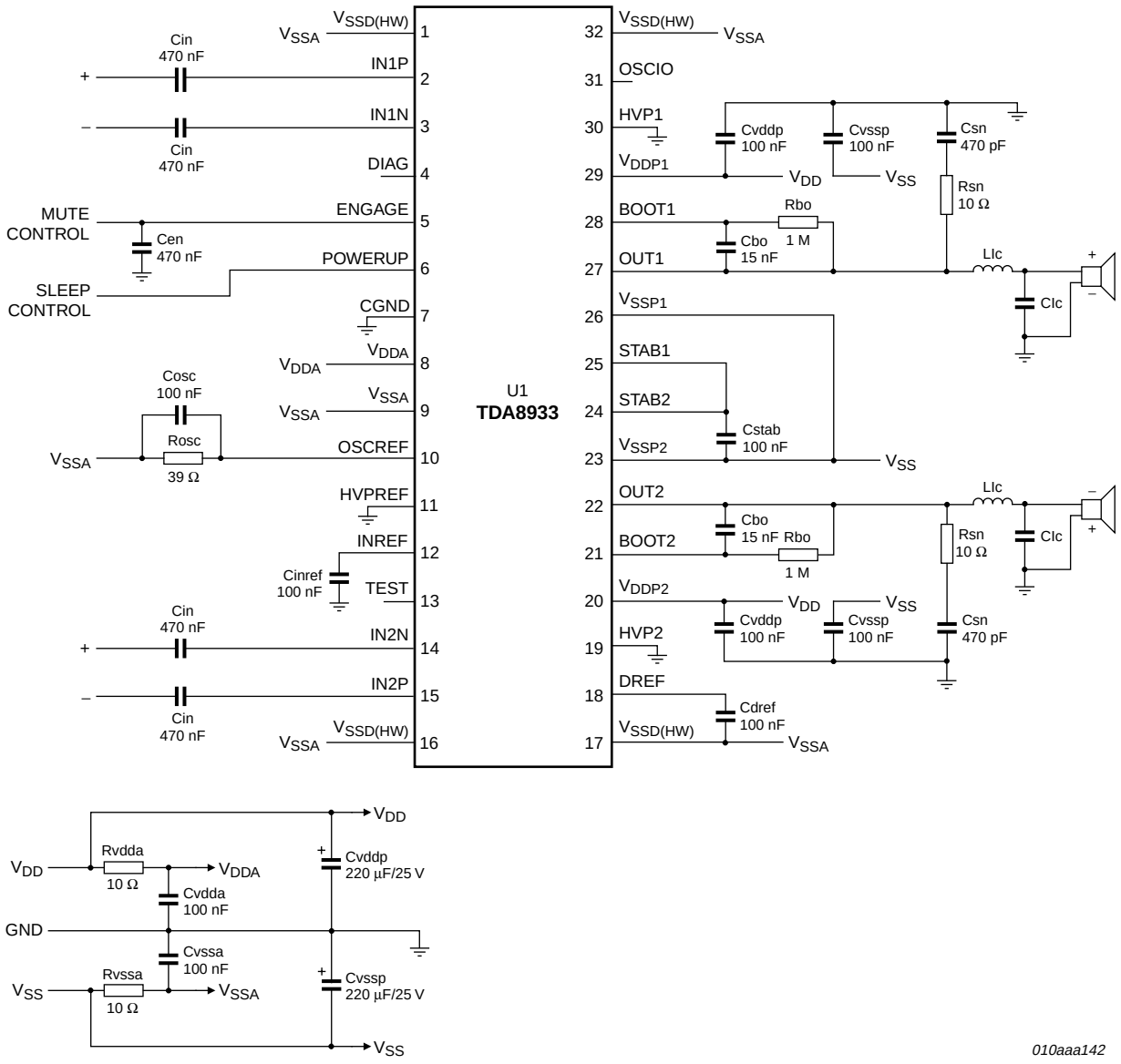


Fig 37. Typical simplified application diagram for 2 × SE (symmetrical supply)

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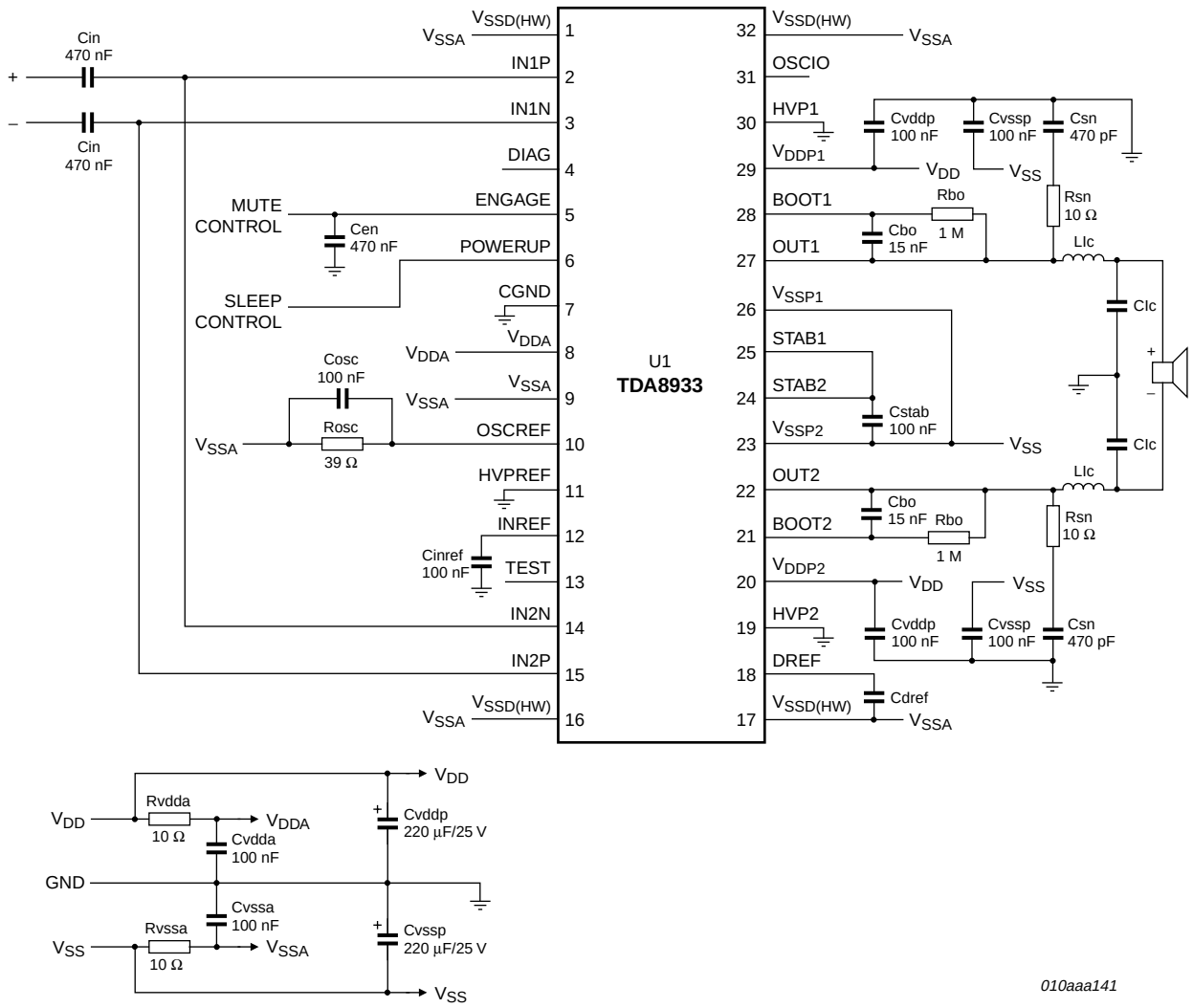


Fig 38. Typical simplified application diagram for 1 × BTL (symmetrical supply)

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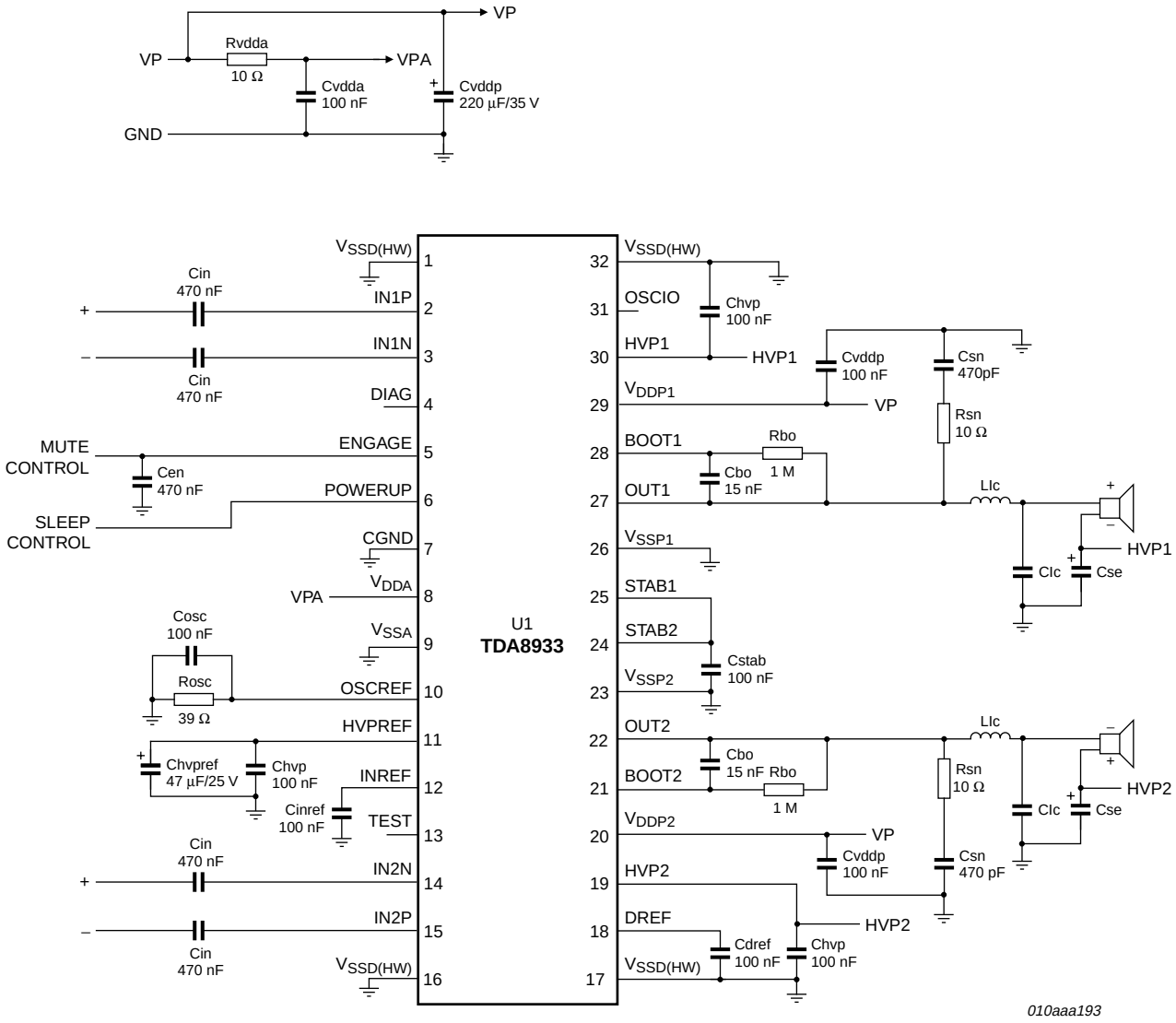


Fig 39. Typical simplified application diagram for 2 × SE (asymmetrical supply)

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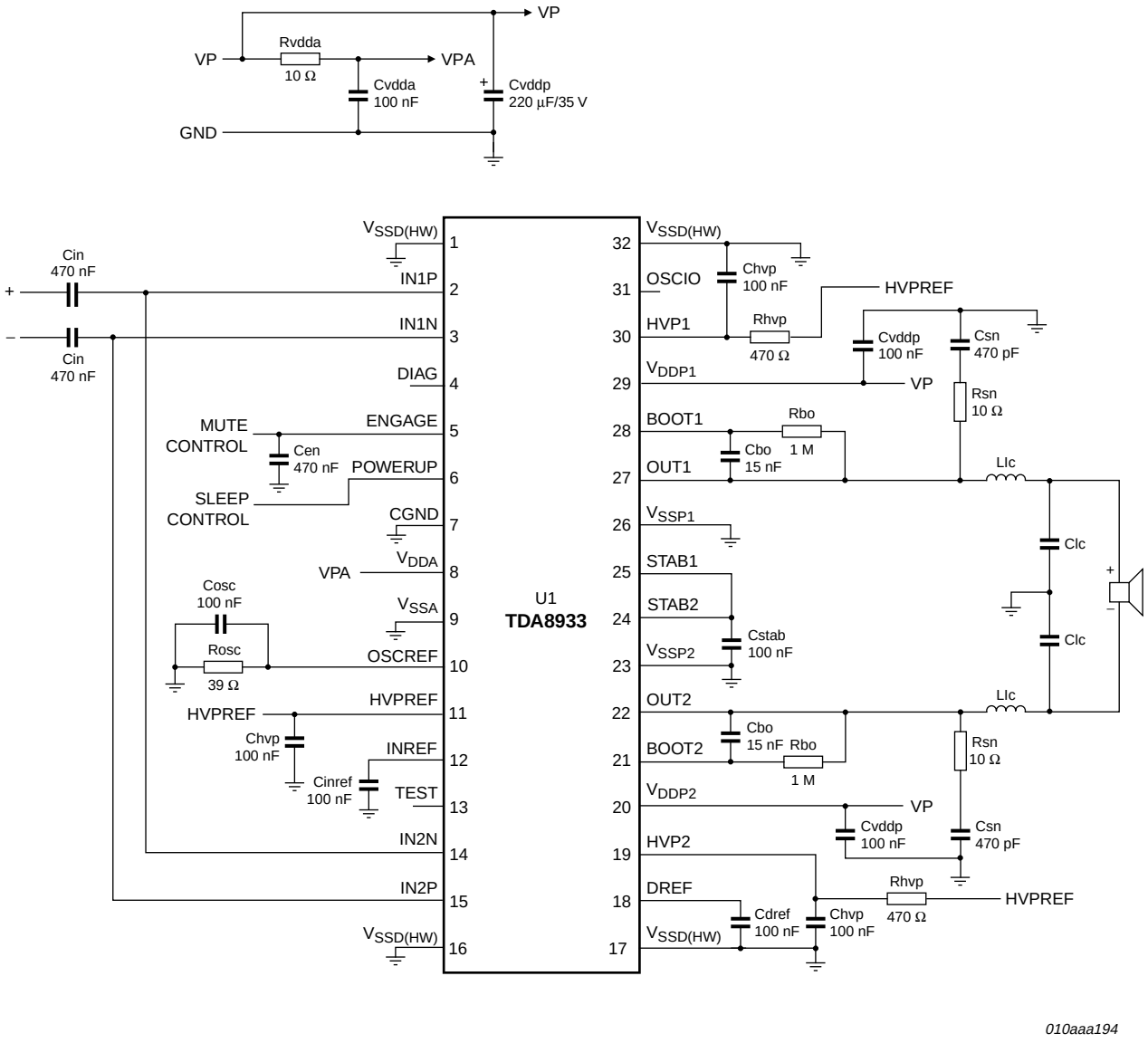
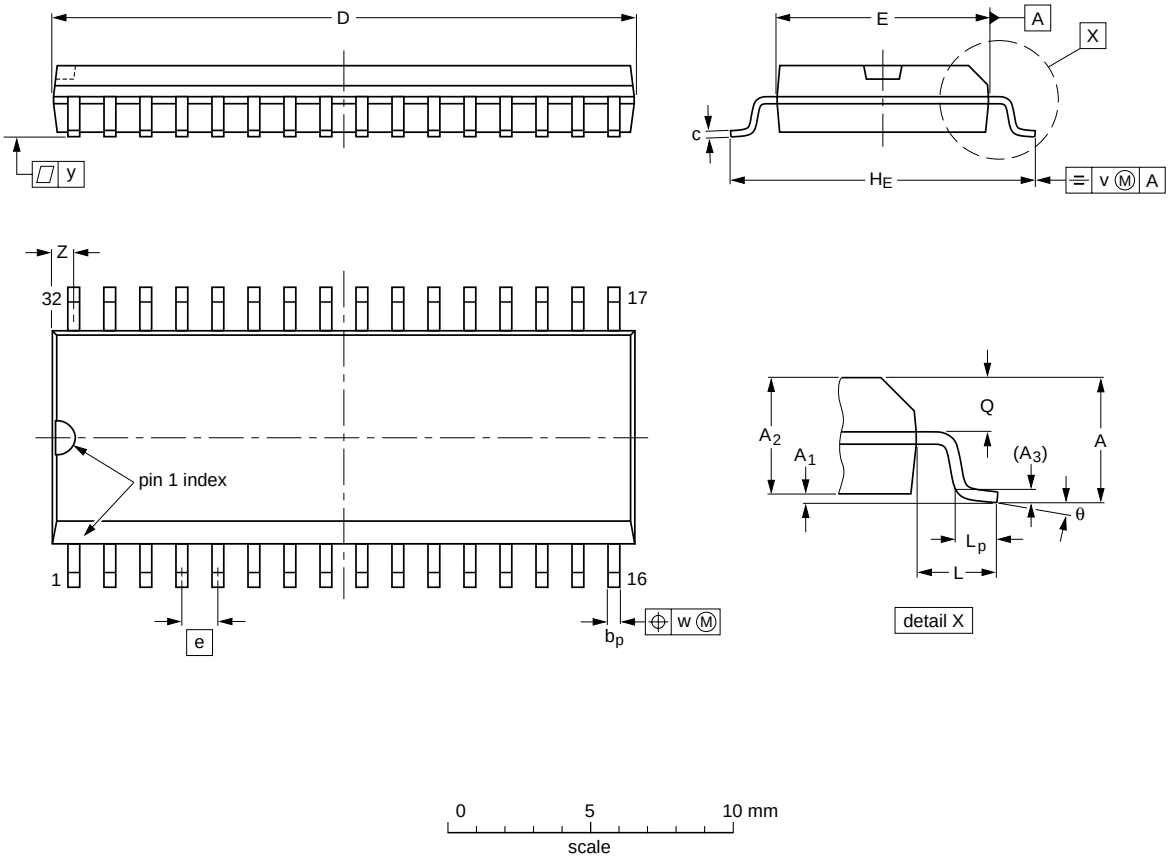


Fig 40. Typical simplified application diagram for 1 × BTL (asymmetrical supply)

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15. Package outline

SO32: plastic small outline package; 32 leads; body width 7.5 mm **SOT287-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.27 0.18	20.7 20.3	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.2 1.0	0.25	0.25	0.1	0.95 0.55	8^o 0^o
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.02 0.01	0.011 0.007	0.81 0.80	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.047 0.039	0.01	0.01	0.004	0.037 0.022	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT287-1		MO-119				~~00-08-17~~ 03-02-19

Fig 41. Package outline SOT287-1 (SO32)

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16. Revision history

Table 16. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TDA8933_1	20070515	Preliminary data sheet	-	-

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17. Legal information

17.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

17.2 Definitions

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